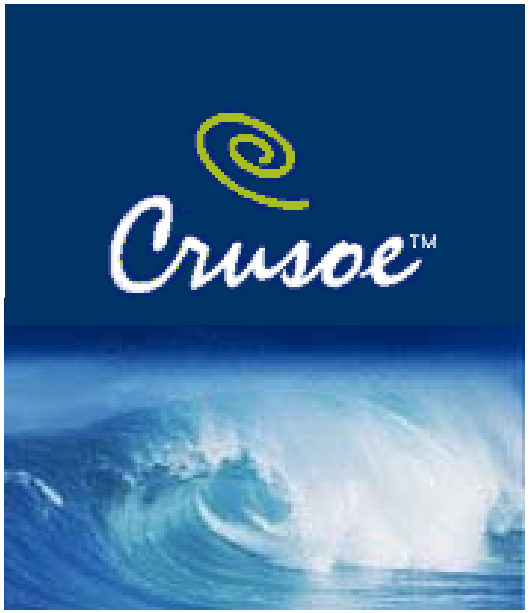
Introducing the Transmeta Efficeon TM8000 Microprocessor Family

Matthew R. Perry, Ph.D.
President and Chief Executive Officer

David R. Ditzel
Co-Founder, Vice-Chairman and CTO

October 14 ,2003

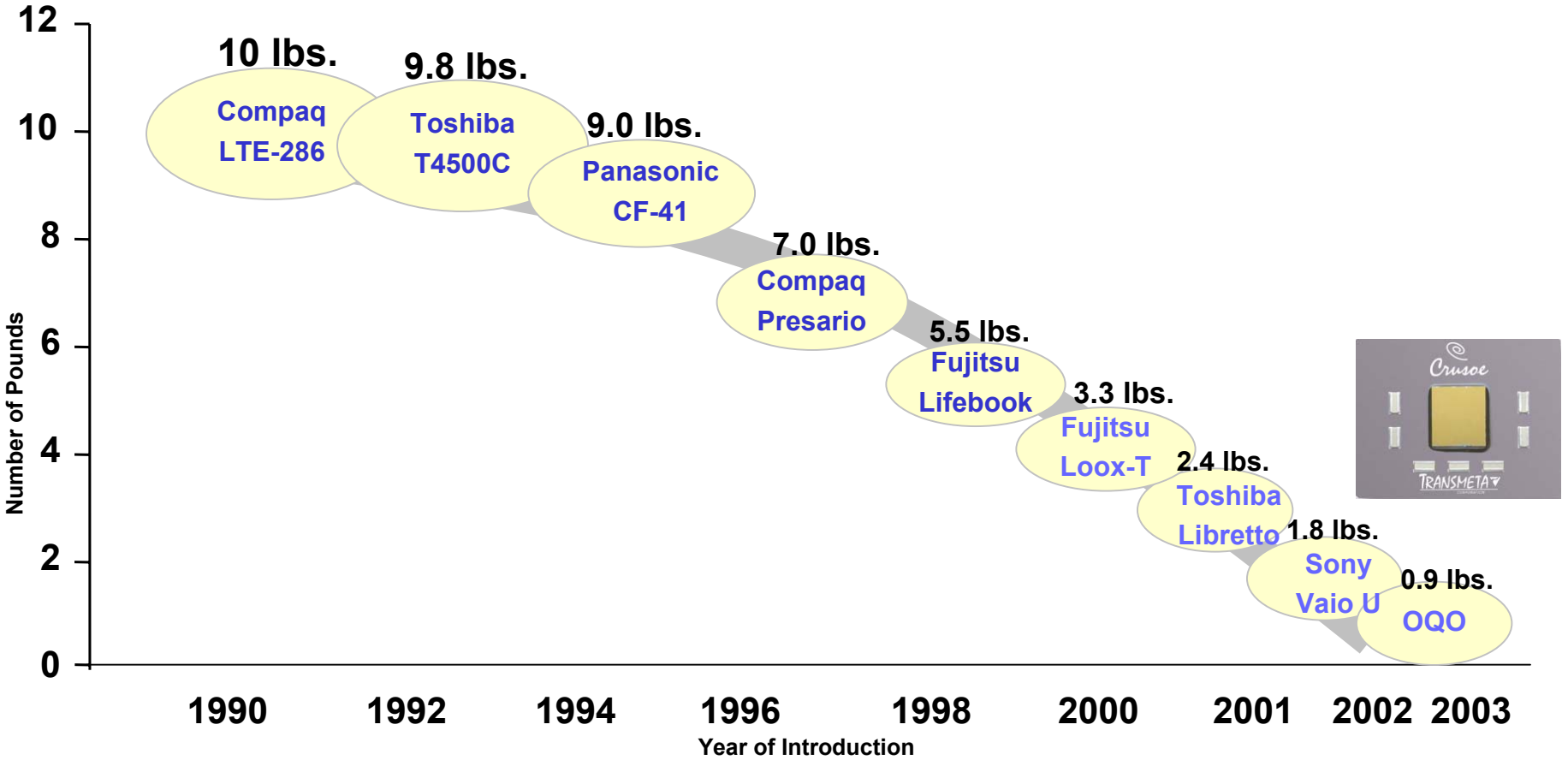
How Crusoe Changed the Industry



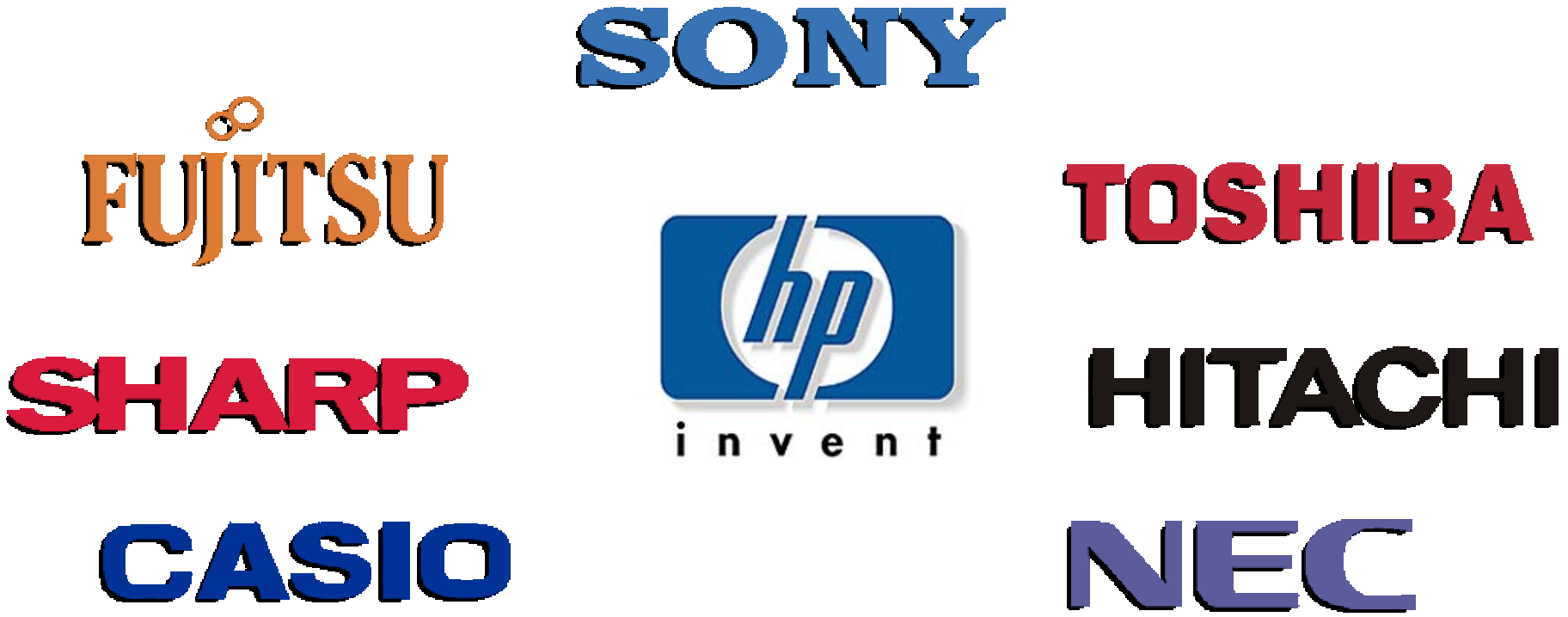
"Until Transmeta released the Crusoe processor in 2000, the mobile computer market was stagnating with repurposed desktop technology, oversized and overweight hardware, and disappointing growth. Crusoe showed the computer industry what was possible…"

Rob Enderle, emerging technology expert for the Enderle Group

Notebook Computer Market Evolution

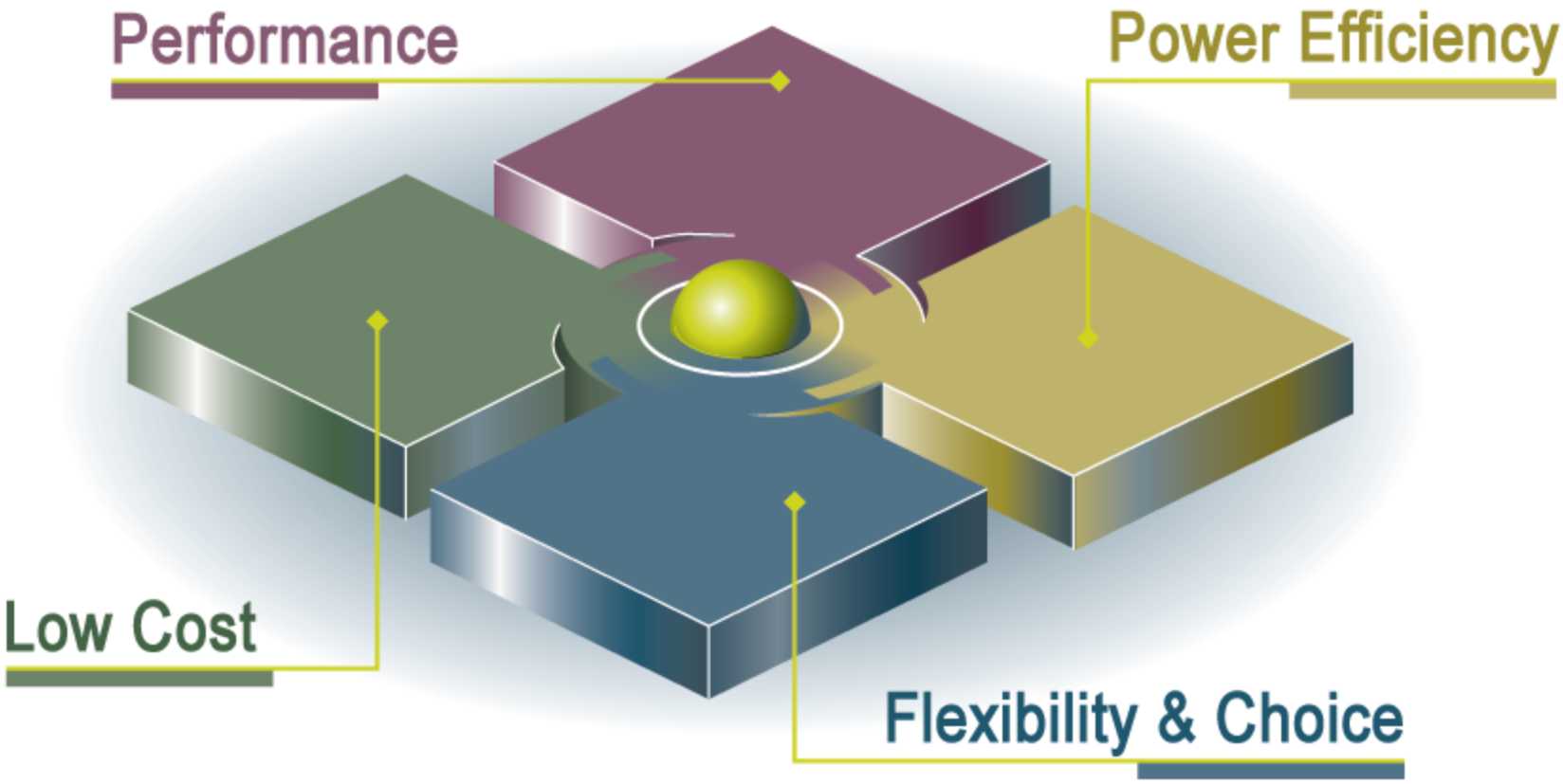


Crusoe Was Adopted by Mobile PC Leaders

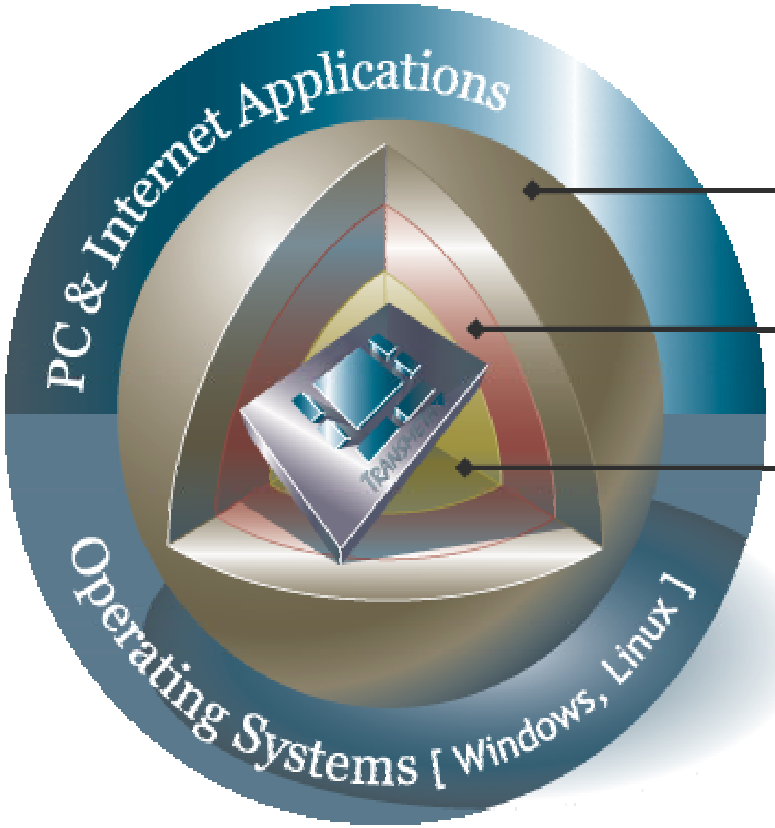


Crusoe was used by 6 of top 10 worldwide leaders!

Transmeta Is A Leading Provider of Efficient Computing Processors



Based on Transmeta's Unique Approach



Code Morphing™ Software

LongRun™ Power Management

VLIW Core

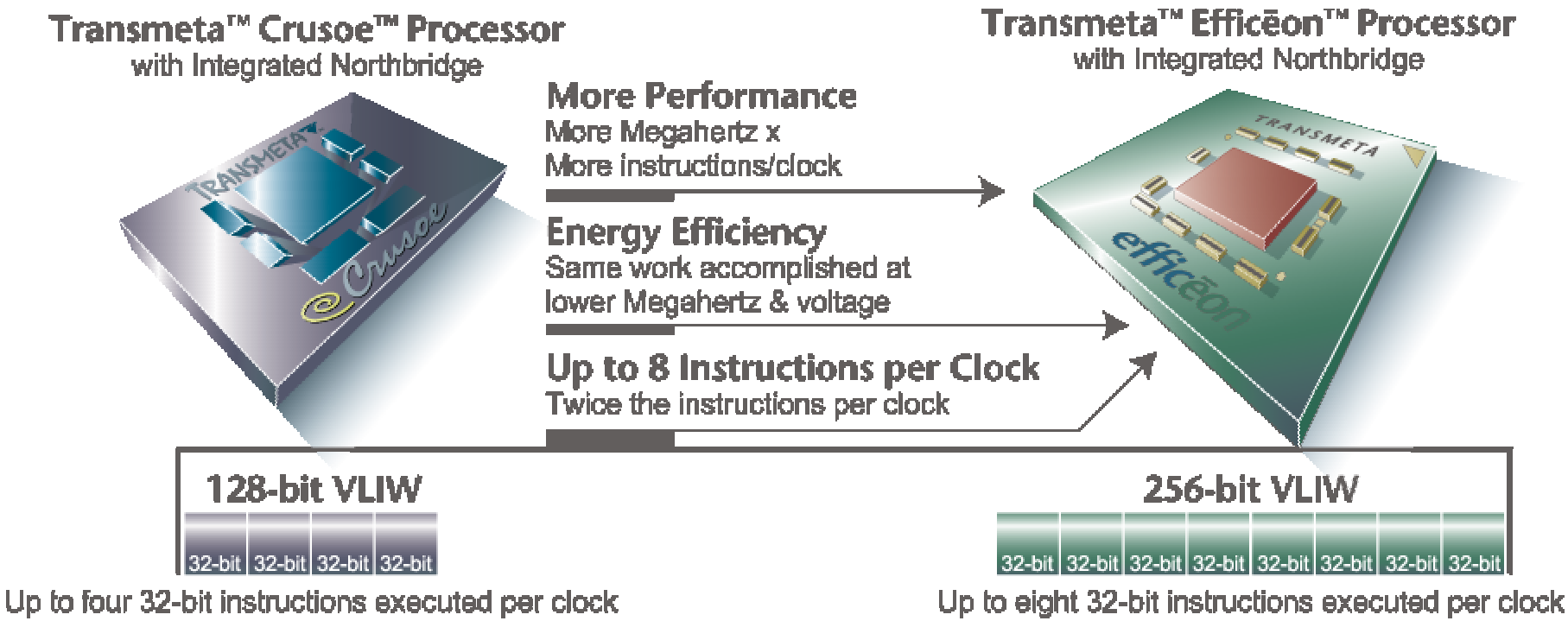
Trades Transistors for Software

A NEW ēon OF efficiency


efficēon

Performance Efficient

More Work Per GHz plus More GHz



efficēon
efficient computing

Wider Market for Efficeon

High End / Performance

Low End / Value

Embedded	Thin Client	UPC	Thin & Light	Mainstream Laptop	Blades & Quiet DT
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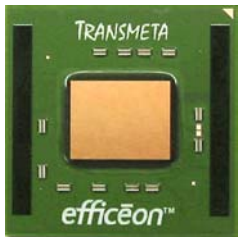
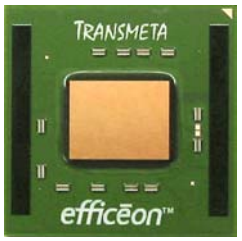
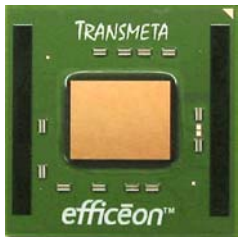
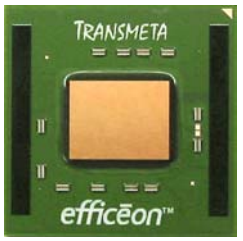
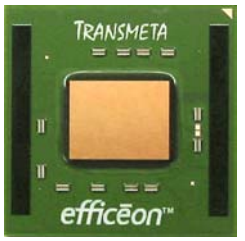
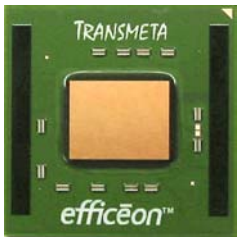
					
Crusoe SE	Crusoe	Crusoe	Cru		
					

Performance

Efficient Computing Overview

Performance Efficient

- Higher performance per cycle, and higher GHz
- Performance comparable or superior to leading competitors

Power Efficient

- Extremely low standby power
- Low power integrated northbridge

Space Efficient

- Two compact packaging options for the microprocessor
- Highly integrated chipsets are also space efficient

Cost Efficient

- Efficeon will lead in x86 “Performance per Watt per Dollar”
- Simpler thermal solution and smaller board save cost

Freedom of Choice

- Enables choice of best-in-class solutions from industry leaders
- Chipset, Graphics, Wireless solutions available today

Industry Endorsements and Thank-You's

Efficeon Endorsement Partners

Efficeon OEM Endorsers

Special Thank-You: Sharp

- Sharp has provided Efficeon-based prototype systems for our technology demonstrations at the launch.
  - These demos can be viewed in the demonstration area.

- *Historical Reference: Sharp's existing Actius MM10 notebook, based on the Crusoe processor, is the thinnest and lightest full-featured notebook computer available for sale in the U.S.*
  - *Sharp's MM10 is Ranked #8 on PC World's Top 15 Notebook PCs ranking for the month of September*.

Sharp's Actius MM10 is based on the Crusoe Architecture

Special Thank-You: Fujitsu

- Fujitsu has provided Efficeon-based prototype systems for our technology demonstrations at the launch.
  - These demos can be viewed in our demonstration room

- *Historical Reference: Fujitsu's LifeBook P Series, which used the Crusoe processor, when introduced, was the world's smallest full featured notebook*

Fujitsu's LIfebook P Series was based on the Crusoe Architecture

Special Thank-You: TSMC

- TSMC is manufacturing the Efficeon family in the same well-proven 130nm process as is currently used to deliver the 1GHz Crusoe

- Has provided outstanding support during the development of the Efficeon processor family
- Provided fast turnarounds for engineering wafers
- Delivered excellent yields
- Proved to be very responsive to Transmeta's needs
- All while meeting their commitments on the 1GHz Crusoe products

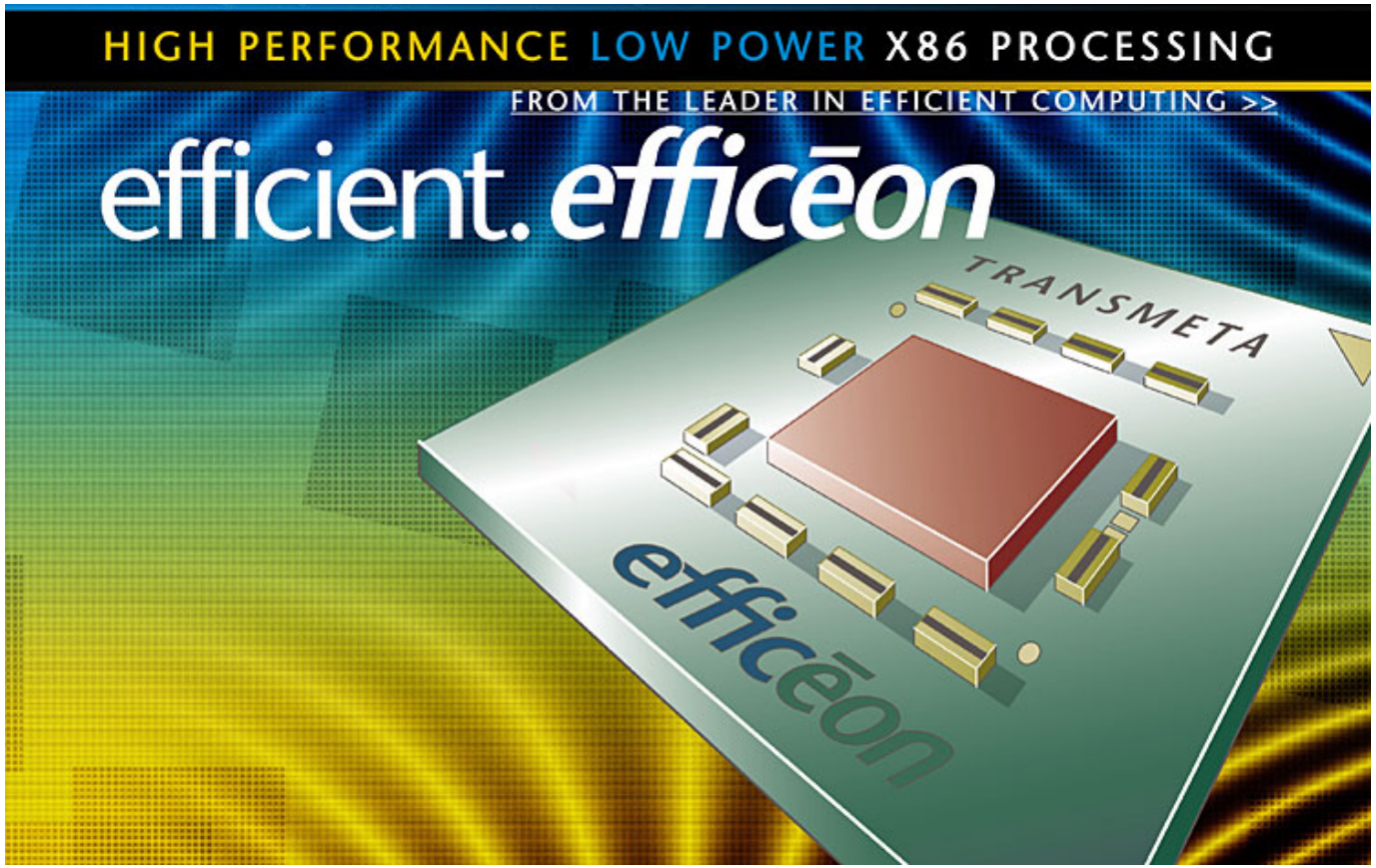
Special Thank-You: Fujitsu Semiconductor

- On October 7th it was announced that Fujitsu Semiconductor had been selected as the 1st foundry for the planned 90nm generation of Efficeon products

- 'Mainframe class' process expected to deliver high clock frequencies based on advanced 90nm transistors with leadership 40nm physical gate lengths
- Close collaboration with Transmeta engineers
- Dedicated engineering resources
- Excellent communications and program management

- ***Production Goal: Second Half 2004***

The New Era Has Begun!



Introducing the Transmeta Efficeon TM8000 Microprocessor

David R. Ditzel
Co-Founder, Vice-Chairman and CTO
Transmeta Corporation

October 14 ,2003
Efficeon Launch Event

Agenda

- **Introducing Efficeon**
- **Efficeon Technical Overview**
  - High Performance IO Interfaces
  - New Code Morphing Software
  - Microarchitecture Description
- **Evaluation**
  - Performance
  - Power
  - Board Area
- **Processor Roadmap**
- **Summary**
- **LongRun2 Technology Preview**

Transmeta is pleased to announce:

A new *eon* for *efficient* PC computing:

Efficeon is…
Transmeta's Next Generation Processor

A high-performance, low-power x86 microprocessor

- New 256-bit VLIW microarchitecture issues up to 8 instructions/cycle
- New Code Morphing Software
- Fully x86 compatible (Pentium-4 ISA)
- Supports MMX / SSE / SSE-II SIMD instructions for multimedia

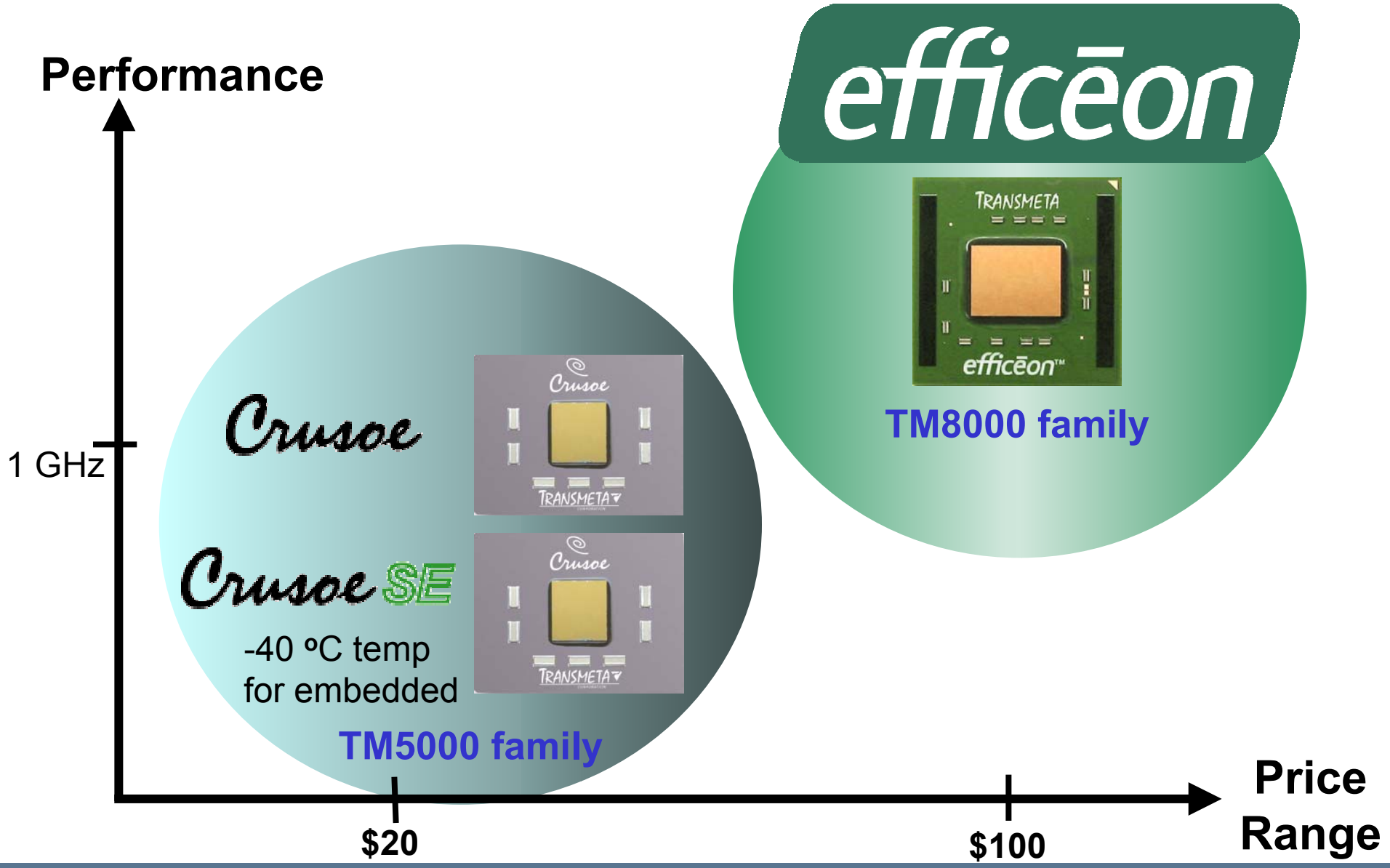
Features an enhanced integrated northbridge

- Integrated DDR Memory interface
- Integrated AGP Graphics interface
- Integrated HyperTransport interface

Efficient Design

- Performance Efficient: Better performance / MHz than Pentium-4
- Energy Efficient: New low power features
- Space Efficient: Small real-estate solutions
- Cost Efficient: Simple design enables low cost manufacturing

Crusoe and Efficeon



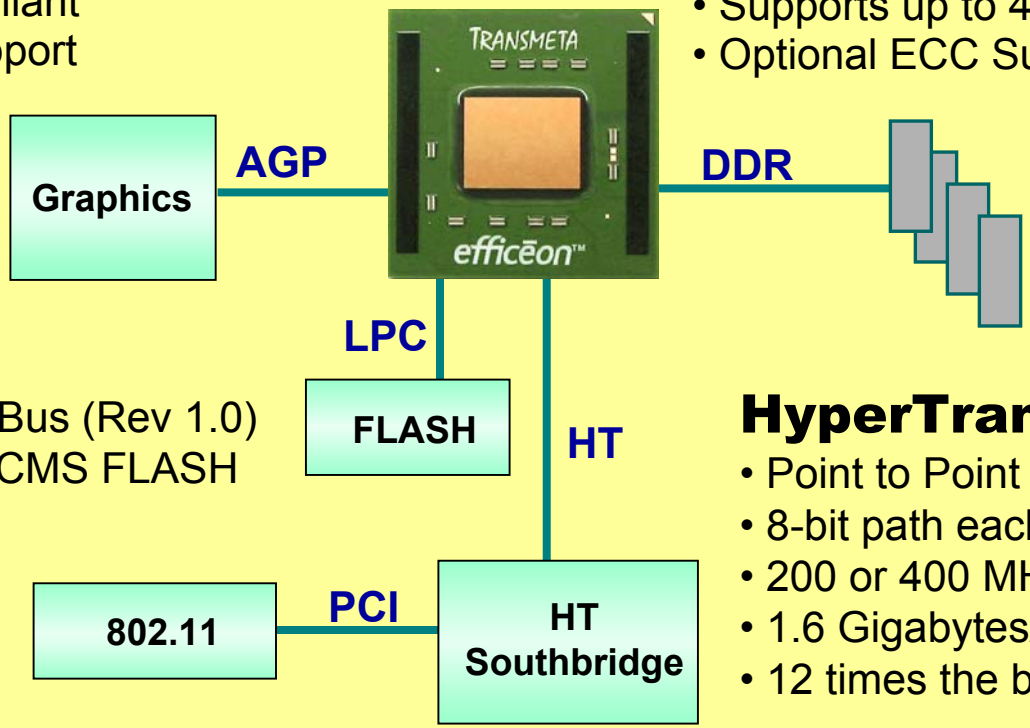
Efficeon: High Performance Interfaces

AGP- 4X Graphics

Supports 1X, 2X or 4X rates
AGP 2.0 compliant
Full GART support

DDR-400 Memory

- High Performance 64-bit DDR
- Up to 200MHz/400 Megatransfers/sec
- Supports up to 4GB of memory
- Optional ECC Support



LPC

Low Pin Count Bus (Rev 1.0)
Used for BIOS/CMS FLASH

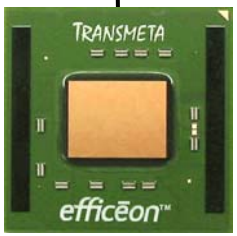
HyperTransport IO

- Point to Point LVDS Interface
- 8-bit path each direction
- 200 or 400 MHz Speeds
- 1.6 Gigabytes/s aggregate
- 12 times the bandwidth of PCI

Support for High Performance Graphics, Memory, and Communications

Transmeta Technology

Efficeon is the sum of

x86 Code Morphing Software + 

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Low Power

x86 PC Compatibility

High Performance

Code Morphing Software

- Provides Compatibility
- Translates the 1's and 0's of x86 instructions to equivalent 1's and 0's for a simple VLIW processor
- Learns and improves with time

VLIW Hardware

- Very Long Instruction Word processor
- Simple and fast
- Fewer transistors

Efficeon: A New Micro-Architecture

An 8 Instruction/Clock CPU for Mainstream PC Use

Crusoe TM5800

CPU with Integrated Northbridge

4 instr/clock to 8 instr/clock

More than twice the Instruction Level Parallelism

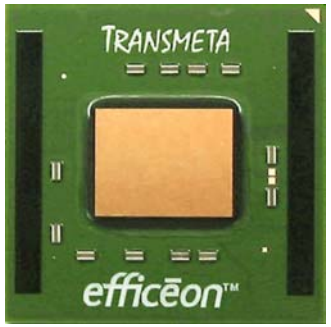
Higher Performance

More MHz x more ILP

Energy Efficiency

Can run same workload at lower MHz and Voltage

Efficeon TM8000



CPU with Integrated Northbridge

128-Bit VLIW

32 Bit	32 Bit	32 Bit	32 Bit

Four 32-bit instructions issued per clock

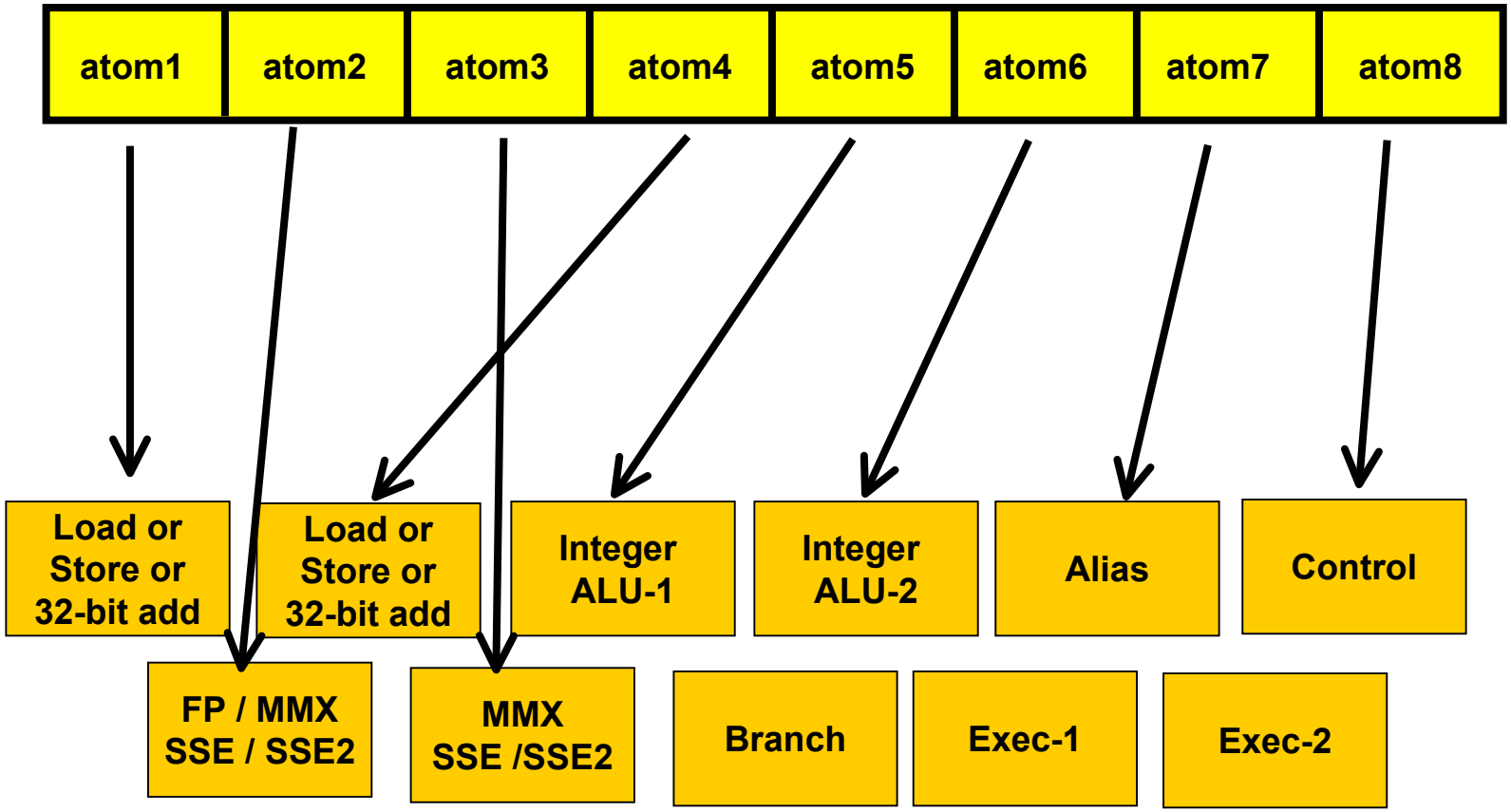
256-Bit VLIW

32 Bit	32 Bit	32 Bit	32 Bit	32 Bit	32 Bit	32 Bit	32 Bit

Eight 32-bit instructions issued per clock

High Instruction Level Parallelism

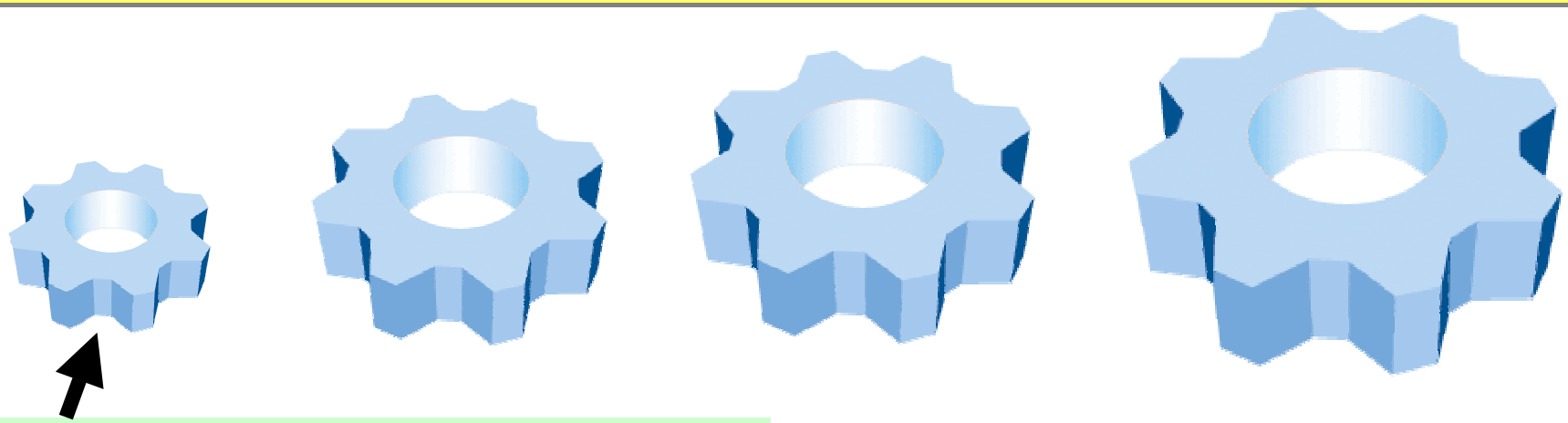
Each clock, Efficeon can issue from one to eight 32-bit instruction "atoms". . .



. . . to any of the above eleven logical execution units.

New Code Morphing Software

4 Gear System Significantly Improves Responsiveness and Overall Performance



1st Gear

Executes 1 instruction at a time

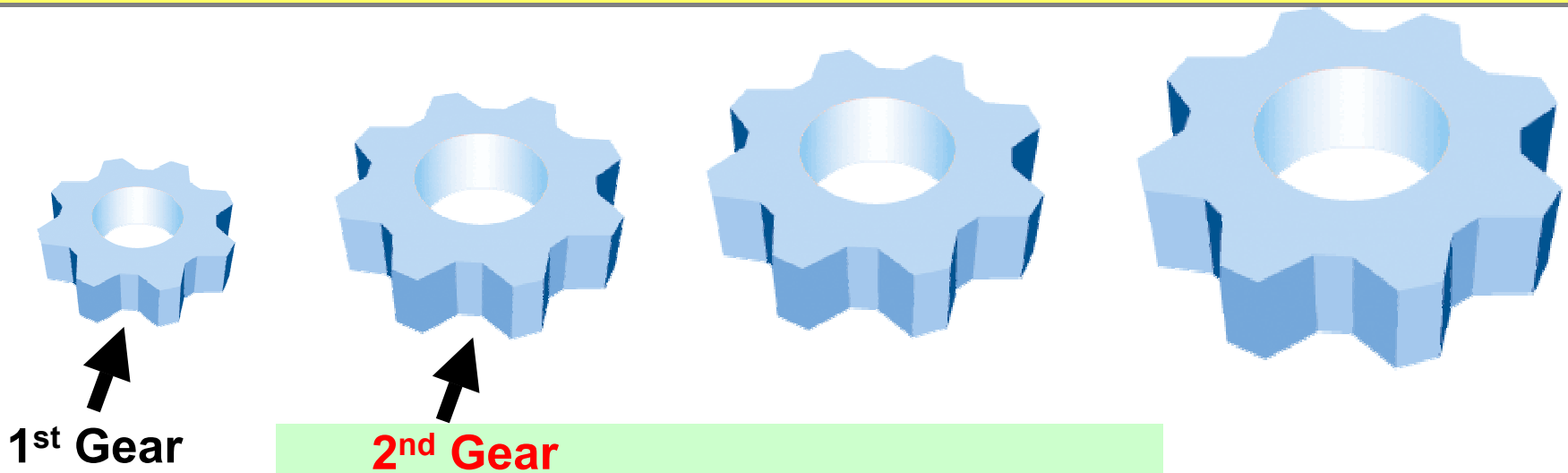
- Profiles code at runtime
- Gathers data for flow analysis
- Gathers branch frequencies and directions
- Detects load/store typing (IO vs memory)

Filters out infrequently executed code

No startup cost
Lowest speed

New Code Morphing Software

4 Gear System Significantly Improves Responsiveness and Overall Performance



1st Gear

2nd Gear

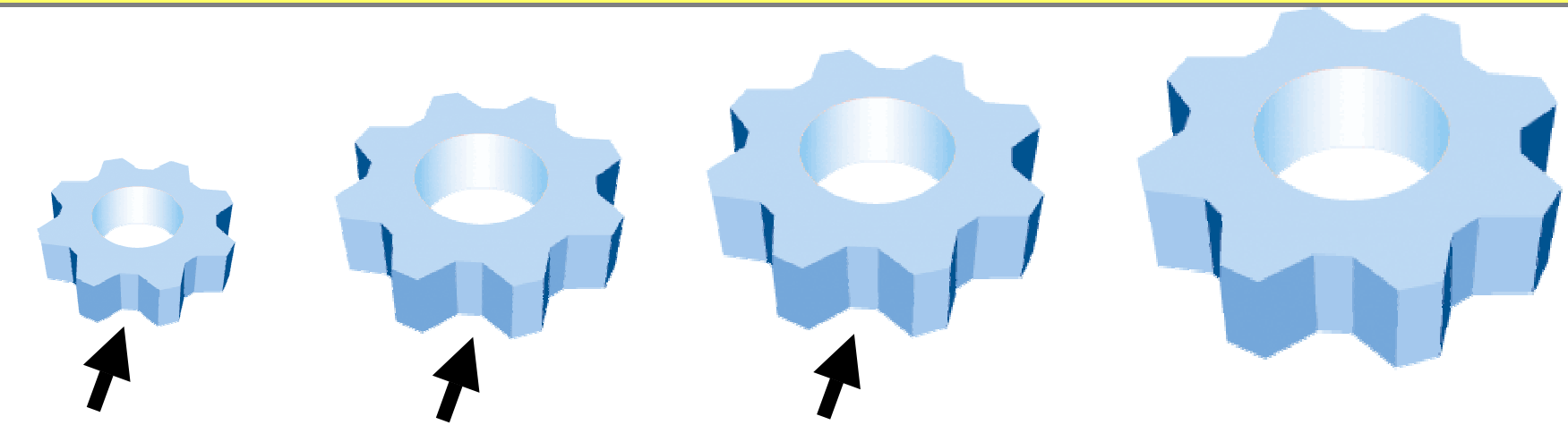
Uses profile data to create initial translations after code reaches 1st threshold.

- Translates a “Region” of up to100 x86 instructions.
- Adds flow graph “Shape” information
- Light Optimization
- “Greedy” scheduling

Low translation overhead
Fast execution

New Code Morphing Software

4 Gear System Significantly Improves Responsiveness and Overall Performance



1st Gear

2nd Gear

3rd Gear

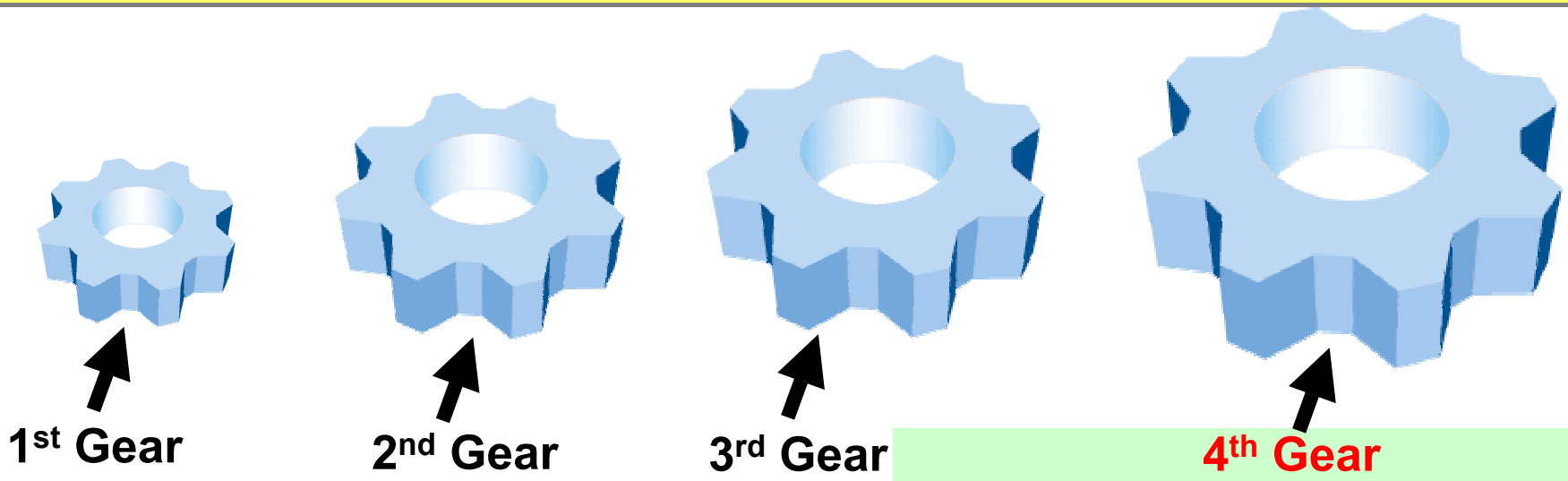
Further optimizes the 2nd gear regions

- Common sub-expression elimination
- Memory re-ordering
- Significant code optimization
- Critical path scheduling

Medium translation overhead
Faster execution

New Code Morphing Software

4 Gear System Significantly Improves Responsiveness and Overall Performance



4th Gear

Most advanced optimizations
for “hottest” code regions.

- Splices together multiple regions
- Optimizes across region boundaries
- Used advanced behavioral data
- Critical path scheduling

Highest translation overhead
Fastest execution

Advanced Code Optimization Capabilities

Some of Efficeon's Advanced Code Morphing Software optimizations:

- Aggressive scheduling of instruction level parallelism for 8-wide VLIW
- Out-of-Order Execution on In-Order Hardware
- Critical path height reduction
- Common sub-expression elimination
- Uses Transmeta's proprietary "Address Alias Checking Hardware"
  - Re-ordering of loads and stores even with potential aliases
  - Elimination of loads and stores even with potential aliases
- Software register renaming to avoid false dependencies
- Fusing operations
- Dead code elimination
- Removal of conditional branches
- Adaptive re-translation during program execution
- Loop unrolling and optimization
  - Remove Exit Branches
  - Code motion across back-edge
  - Loop invariant code motion
  - Strength reduction

Important "hot" codes get the most optimization

Internal Registers and Cache

Registers with support for speculative "Undo/Commit"

- 64 32-bit integer registers
  - 48 shadowed
- 64 80-bit floating point registers
  - Full MMX and SSE-I and SSE-II support
  - 48 shadowed
- 4 Predicate Registers (all shadowed)

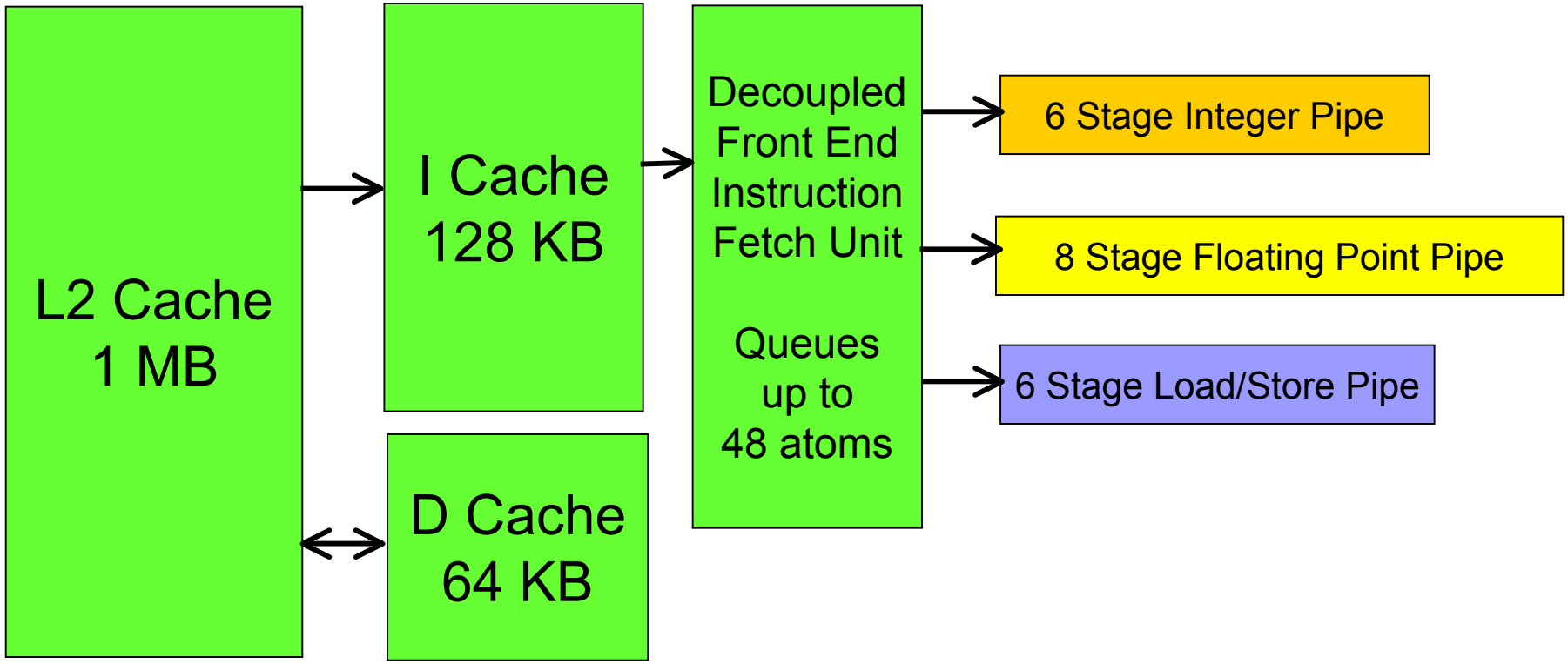
Caches:

- 1 MB Level 2 cache with ECC
  - 4-way set associative, 128-byte lines
- 128 KB Level 1 Instruction Cache
  - 4-way set associative, 64-byte lines
- 64 KByte Level 1 Data Cache
  - 8-way set associative, 32-byte lines

Memory Enhancements with support for speculative "Undo/Commit"

- 14 entry Write Queue / Store Buffer
- 32 entry Victim Cache with 32-byte lines
- 4 32-byte Write combiners
- Support for speculative stores in data cache

VLIW Pipeline Instruction Flow

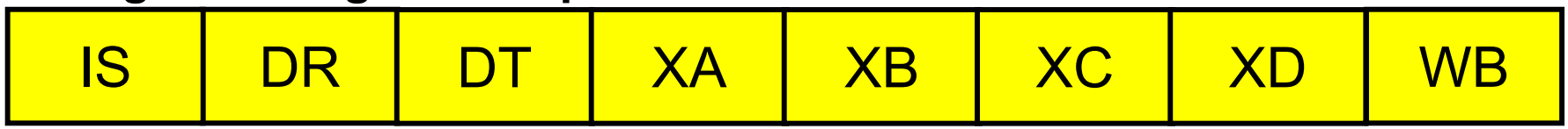


Pipeline Diagrams

6-Stage Integer Pipe

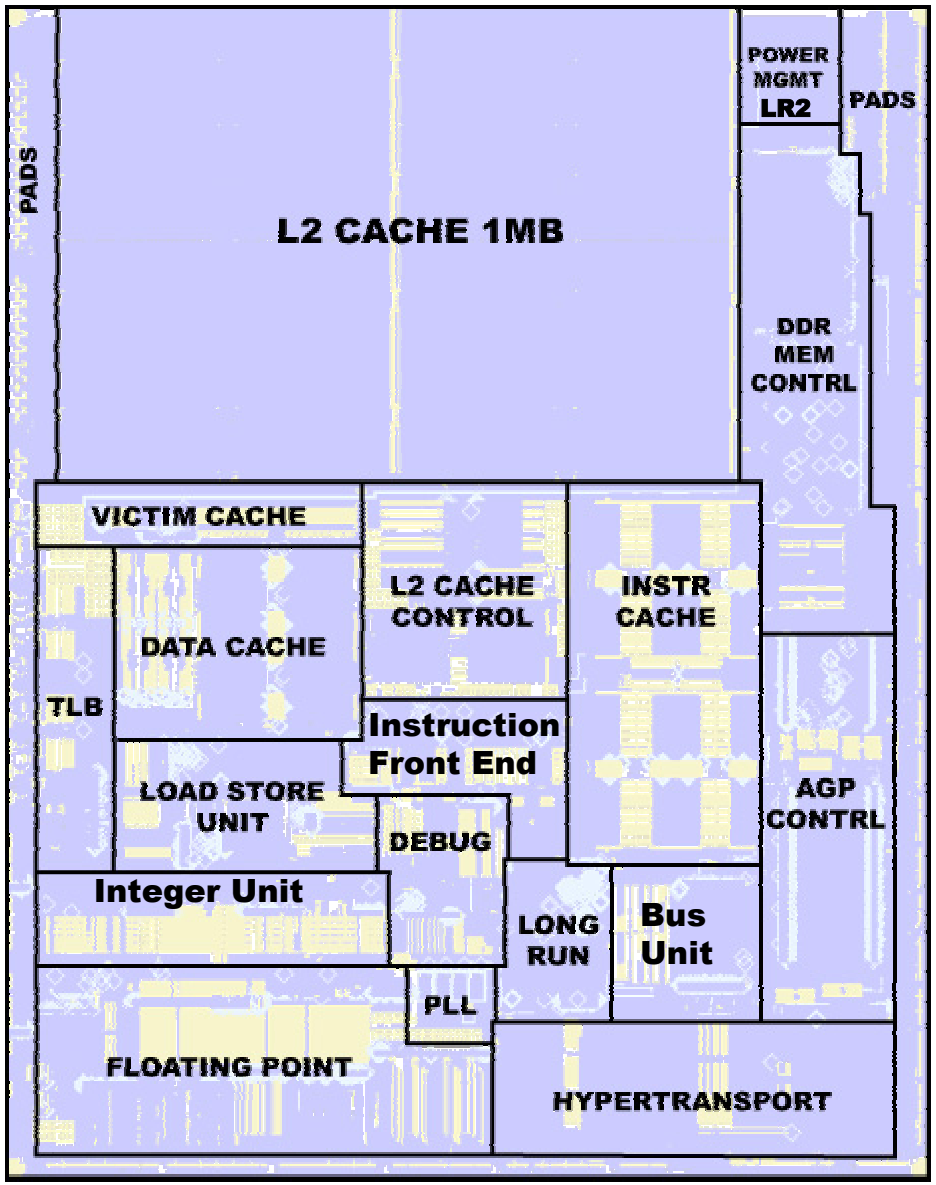
IS: Instruction Issue
DR: Instruction Decode
RM: Register Read for ALU operands
EM: Execute ALU operation
CM: ALU Condition flag completion
WB: Write Back results to integer register file

8-Stage Floating Point Pipe



IS: Instruction Issue
DR: Decode-1
DT: Decode-2
XA: Floating Point compute stage-1
XB: Floating Point compute stage-2
XC: Floating Point compute stage-3
XD: Floating Point compute stage-4
WB: Write Back to floating point register file

Efficeon Processor Layout



Efficeon die size includes Northbridge and AGP Port:

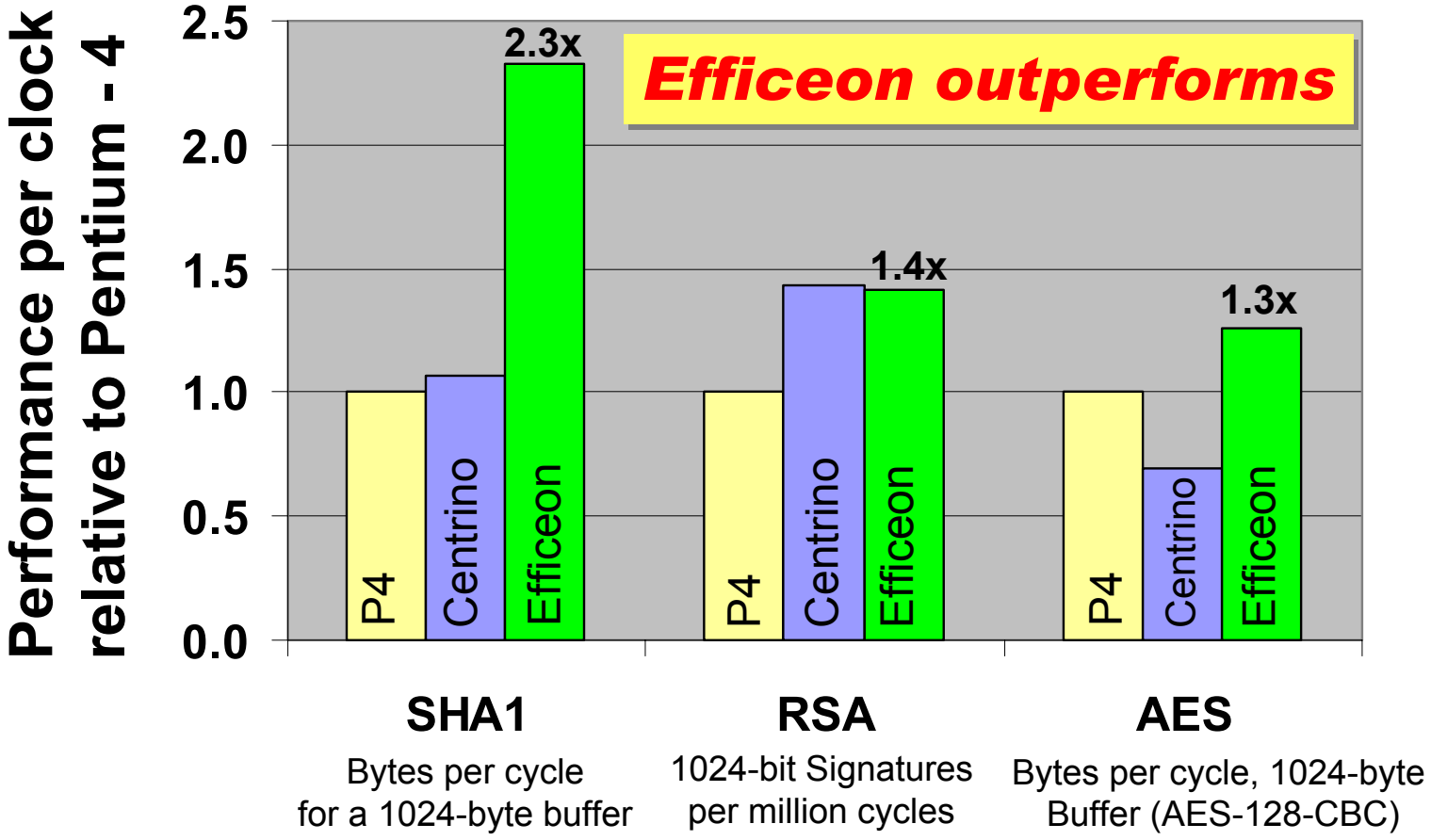
130 nm technology:
119 mm^2 die size

90 nm technology:
68 mm^2 die size

Performance

Integer Performance per Clock

SHA1, RSA and AES are the basis for modern encryption suites, and are a good real-world benchmark of computationally intensive integer codes.



Comparing Mobile Performance

TDP = maximum Thermal Design Power

- For many form factors, TDP often limits the maximum MHz
- 7 Watts TDP tends to be about the upper limit for fanless notebook systems

What MHz can you achieve within a 7 Watt TDP?

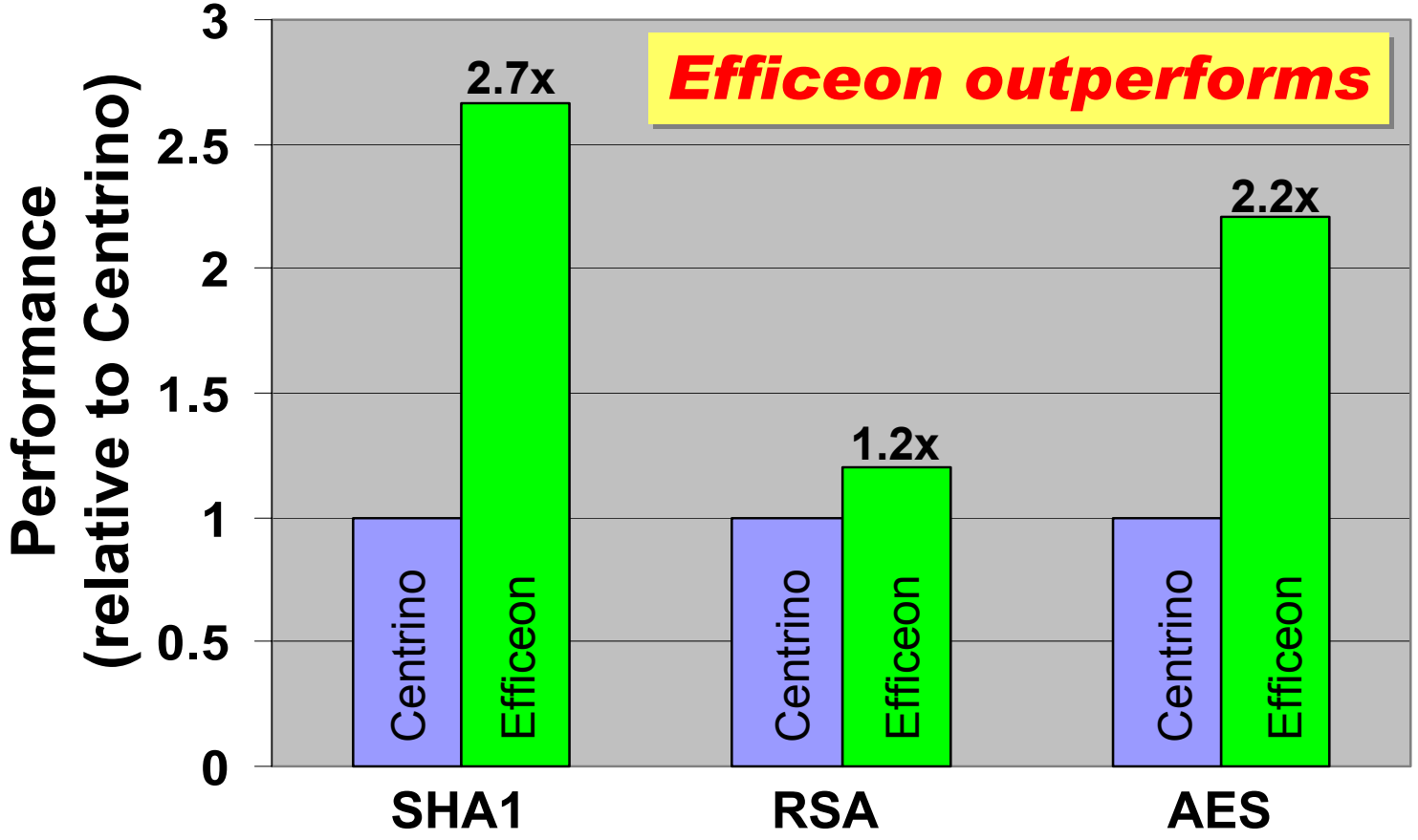
- Different processors achieve different MHz for the same TDP limit
- To compare performance, you must compare at the maximum MHz for a given TDP limit

For example, maximum MHz for the common 7W TDP envelope:

Intel Centrino	Transmeta Efficeon
7 Watt TDP	7 Watt TDP
900 MHz	1100 MHz

Integer Performance (at 7 Watt TDP MHz)

SHA1, RSA and AES are the basis for modern encryption suites, and are a good real-world benchmark of computationally intensive integer codes.



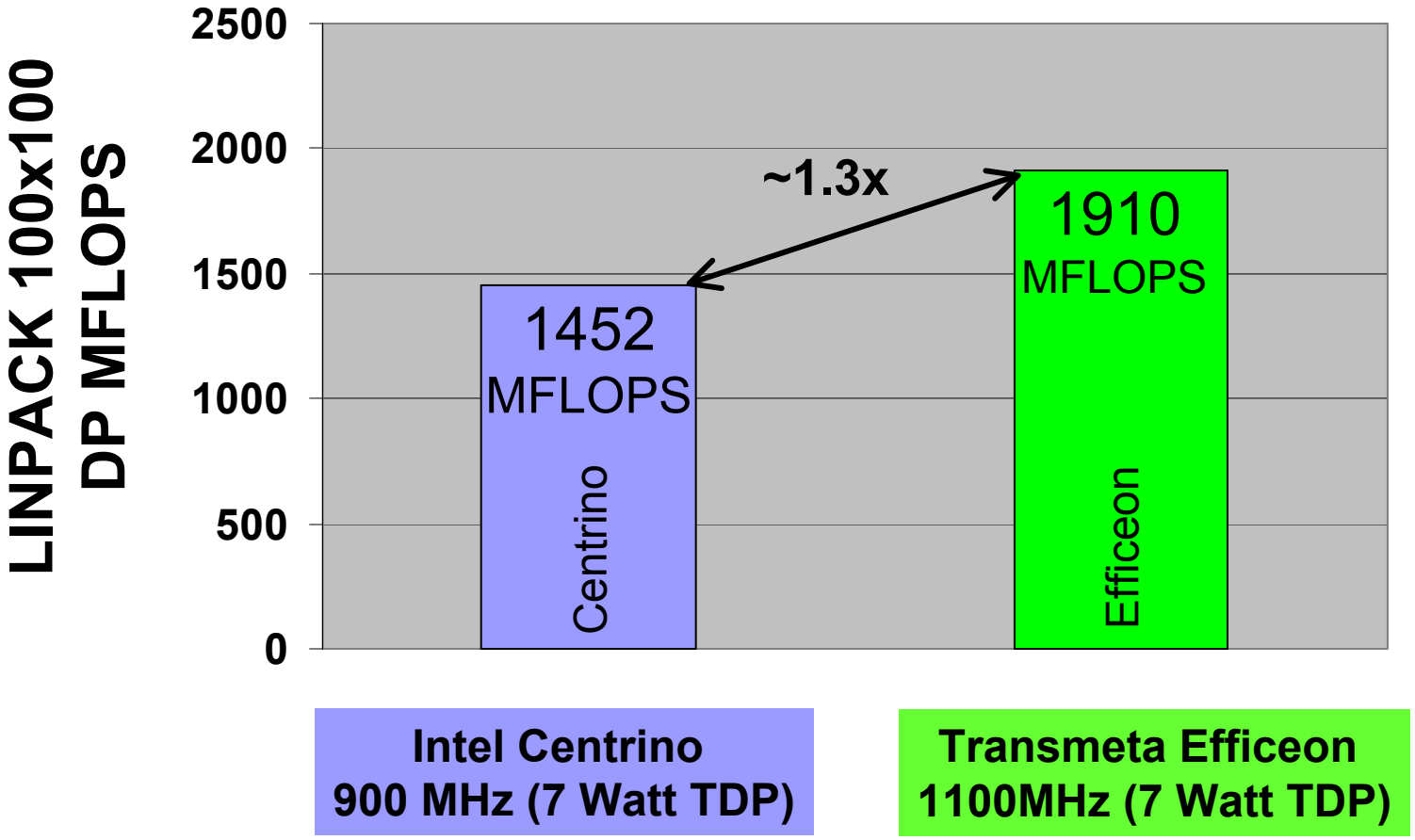
Note: Now relative to Centrino, since there is no 7 watt Pentium-4.

Intel Centrino 900 MHz (7 Watt TDP)

Transmeta Efficeon 1100MHz (7 Watt TDP)

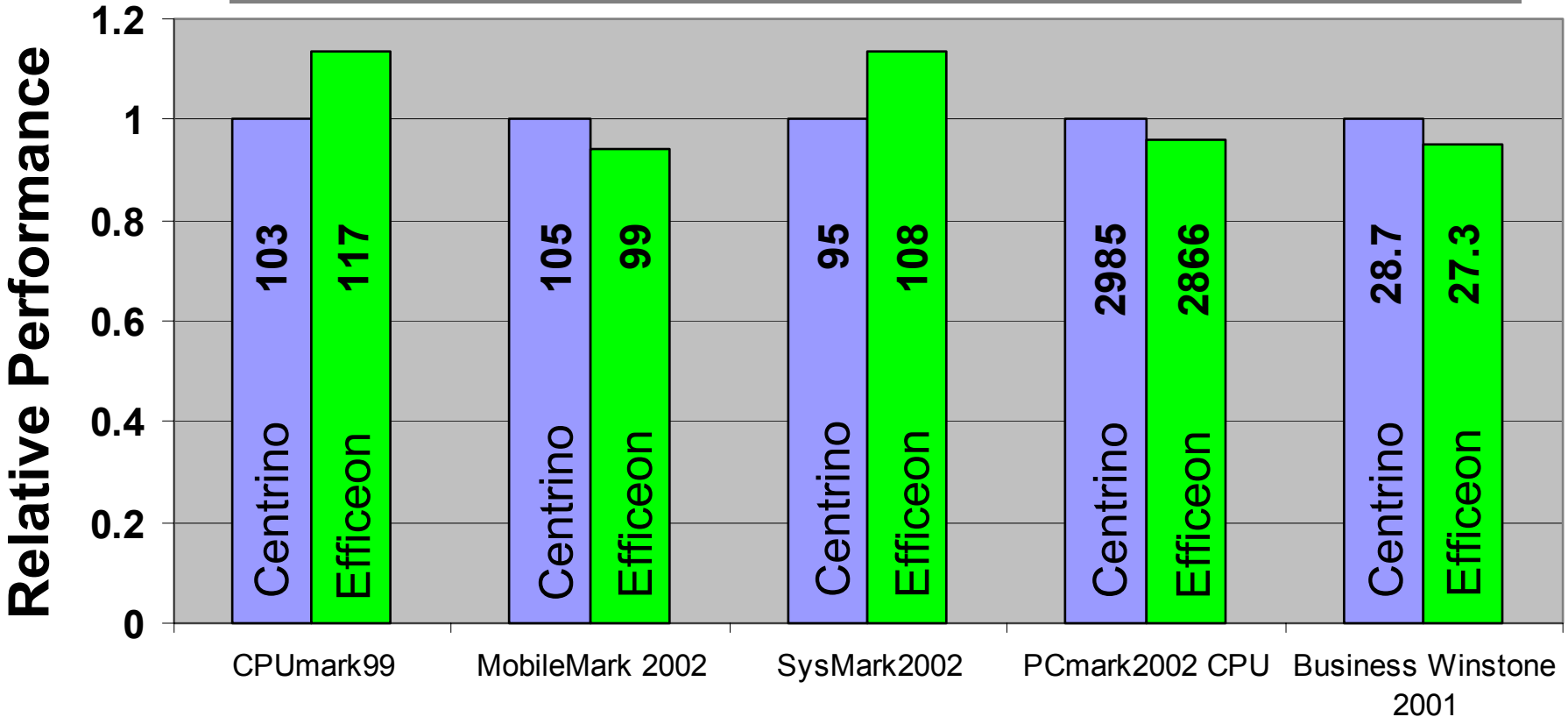
Floating Point Performance (at 7 Watt TDP MHz)

Efficeon outperforms



PC System Performance (at 7 Watt TDP MHz)

Efficeon comparable with system effects



Centrino 900 MHz ~ 7 W TDP
855GM Northbridge ~ 1-2 W TDP

Efficeon 1100 MHz ~7W TDP
(includes integrated Northbridge)

* Similarly configured ultralight systems: DDR-266 DRAM, 1.8" HDD, Windows XP Professional

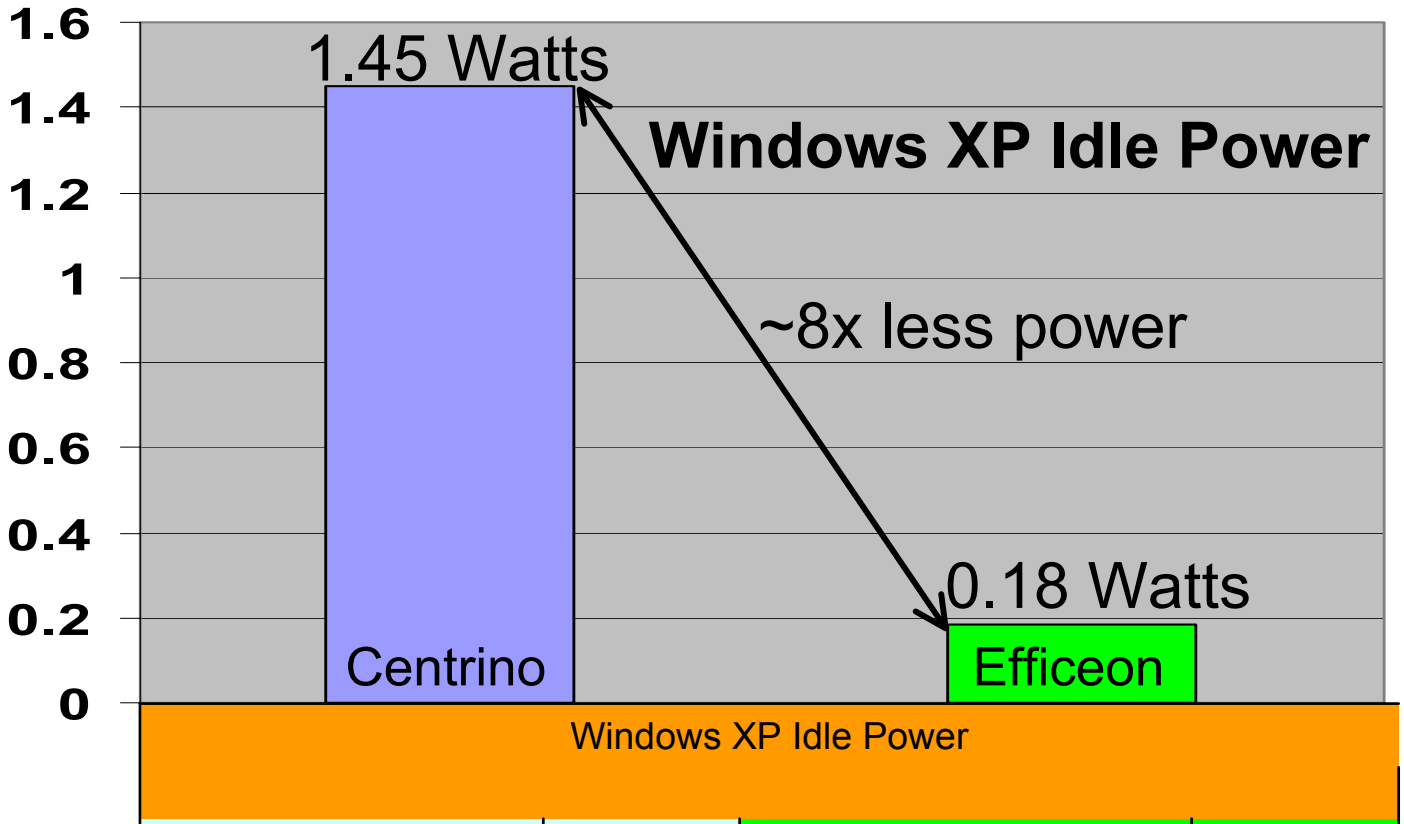
Standby Power

Efficeon consumes ~8x Lower Idle Power CPU + Northbridge + DRAM

Standby power is key for preserving battery life.

Closest *"apples-to-apples"* comparison is to compare key components of

- **CPU Core**
- **CPU IO**
- **Northbridge Co**
- **Northbridge IO**
- **DRAM**

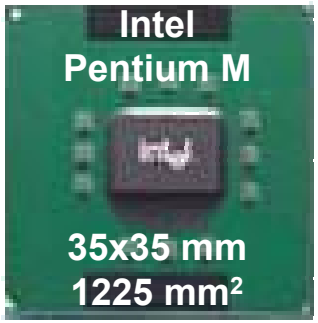


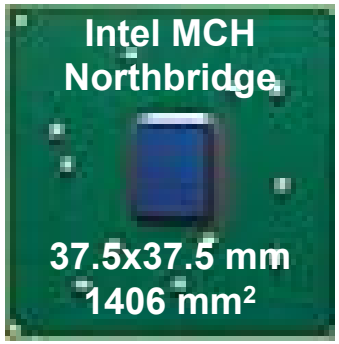
Centrino System Function	Centrino Watts	Efficeon System Function	Efficeon Watts
CPU Core Power	0.275	CPU+Northbridge Core Power	0.055
Front Side Bus Power	0.097	HyperTransport Bus Power	0.073
Northbridge Core Power	0.537		
DDR Memory + NB Bus Power	0.542	DDR Memory + NB Bus Power	0.056
Total CPU+NB+Memory	1.451	Total CPU+NB+Memory	0.184

Measured in comparable systems using supply voltages from each rail to subsystem components. DRAM and Northbridge share a supply.

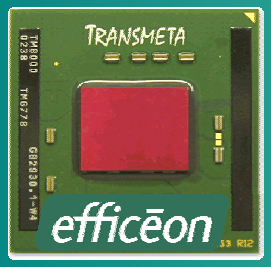
Compact Board Space Solutions from Transmeta and nVidia

Small Package Solutions

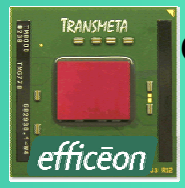




Total Area = 3592 mm²



Efficeon TM8600
CPU + Northbridge
Standard Package
29x29 mm
841 mm²



Efficeon TM8620
CPU + Northbridge
Small Package
21 x 21mm
441 mm²

nVidia
nForce3 Go 150
Southbridge
Standard Package
35x35 mm
1225 mm²

nVidia
nForce3 Go 120
Southbridge
Small Package
22x22mm
484 mm²

Total Area = 2066 mm²

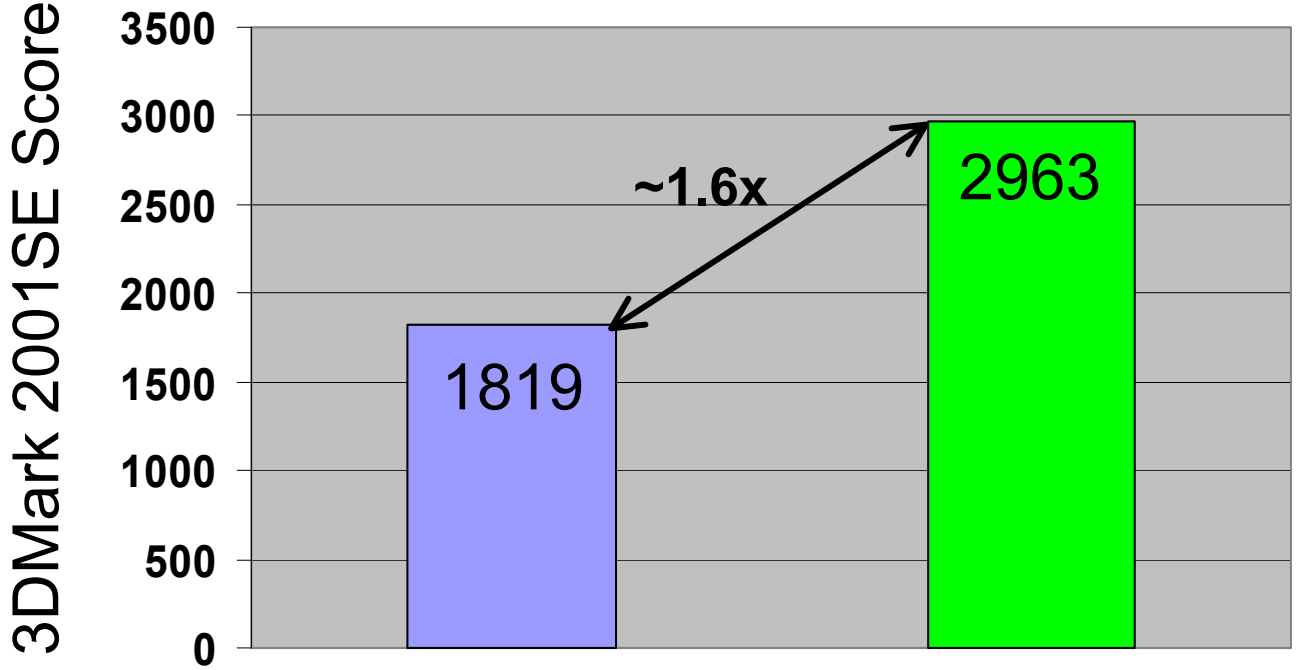
Total Area = 925 mm²

Transmeta CPU+NB & nVidia SB real estate up to 4x smaller

(Figures approximately to scale)

3D Graphics Performance (3DMark 2001)

Efficeon + Nvidia solution outperforms while delivering most compact board area



Intel Centrino 900 MHz
Intel 855GM graphics

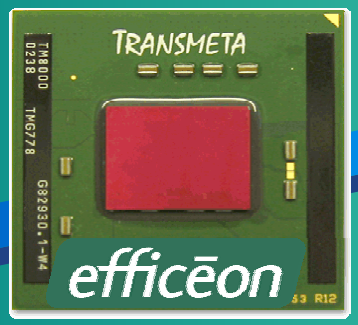
Transmeta Efficeon 1100MHz
nVidia GeForce4 420 Go
nVidia Southbridge

* Resolution for both systems was set to 1024 x 768 x 32. Both CPU's at their 7 Watt TDP MHz limit.

Efficeon Roadmap

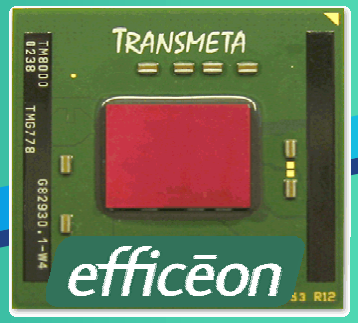
Long Term Efficeon Roadmap
Clock Speed and TDP Maximum Power

Legend:
GHz / TDP Max



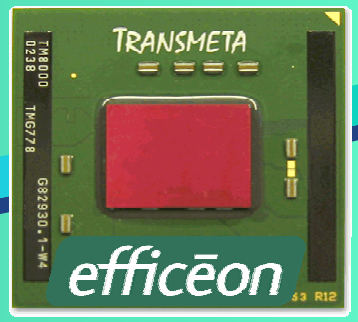
Efficeon Generation-1
TSMC 130 nm

1.3 GHz / 14 W
1.2 GHz / 12 W
1.1 GHz / 7 W
1.0 GHz / 5 W



Efficeon Generation-2
Fujitsu 90 nm

2.0 GHz / 25 W
1.8 GHz / 12 W
1.6 GHz / 7 W
1.4 GHz / 5 W
1.0 GHz / 3 W



Efficeon Generation-3
90/65 nm

Higher Performance
Extended Power Range
New Features

Q4 2003 — **2004** — **2005**

Note: Average power is typically far lower than TDP power.

Efficeon Family Products

There will be a family of Efficeon TM8000 products:

130 nm CMOS Technology

- **TM8600** 1MB L2 Cache — *Standard Package*
- **TM8300** 512KB L2 Cache — *Lower Cost*

- **TM8620** Small Package, 1MB L2 — *Small Size*

90 nm CMOS Technology

- **TM8800** 1MB L2 Cache — *Standard Package*
- **TM8500** 512KB L2 Cache — *Lower Cost*

- **TM8820** Small Package, 1MB L2 — *Small Size*

Summary

Efficeon incorporates all the learning from Crusoe experience

- New microarchitecture and Code Morphing Software
- New high performance interfaces: AGP, DDR, and HyperTransport

Efficeon is a major leap forward in CPU performance.

At comparable thermal limits of nearest competitor, Efficeon is:

- ~2x higher performance on Integer intensive codes AES, SHA1
- ~1.3x higher performance on Floating Point with Linpack
- ~1.6x higher performance on 3D graphics (vs Centrino with 855GM)

Transmeta with nVidia offer extremely compact solutions

- ~4x smaller than closest alternative CPU + Northbridge + Southbridge
- Enables smaller systems, more features, or more battery

Efficeon's leading performance/watt/dollar will allow it to enter

- Mainstream notebooks
- Quiet fanless designs
- Blade servers
- Small mobile systems

Guest Speaker

Transmeta is pleased to have a guest speaker, Dr. Takayasu Sakurai, a world renowned expert in the field of semiconductor technology. Transmeta asked him to summarize one of his recent talks.
His talk will be done by video tape.

Takayasu Sakurai received the Ph.D. degree in EE from the University of Tokyo in 1981. In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, Digital Signal processors, and System-on-a-chip solutions.

From 1988-1990, he was a visiting researcher at the University of California Berkeley.

Since 1996, he has been a professor at the University of Tokyo, working on low-power VLSI, memory design, interconnects, and wireless systems.

He has published more than 250 technical papers including more than 50 invited talks and papers, several books and holds more than 50 patents.

The Future of Semiconductors:

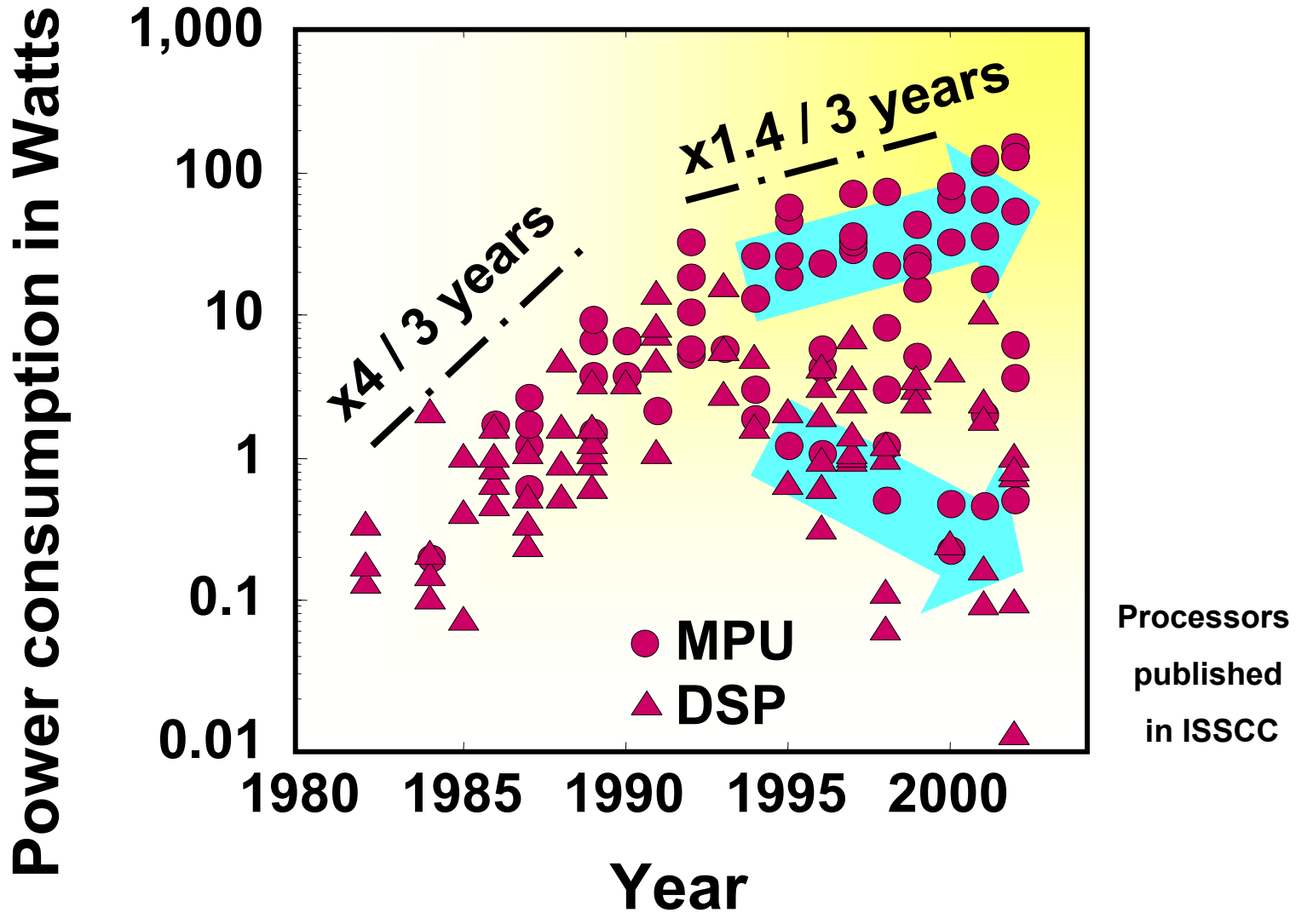
Crises in 90-nanometer technology and beyond

Professor Takayasu Sakurai, Ph.D.
Head of Sakurai Laboratory
Institute of Industrial Science
University of Tokyo
Tokyo, Japan

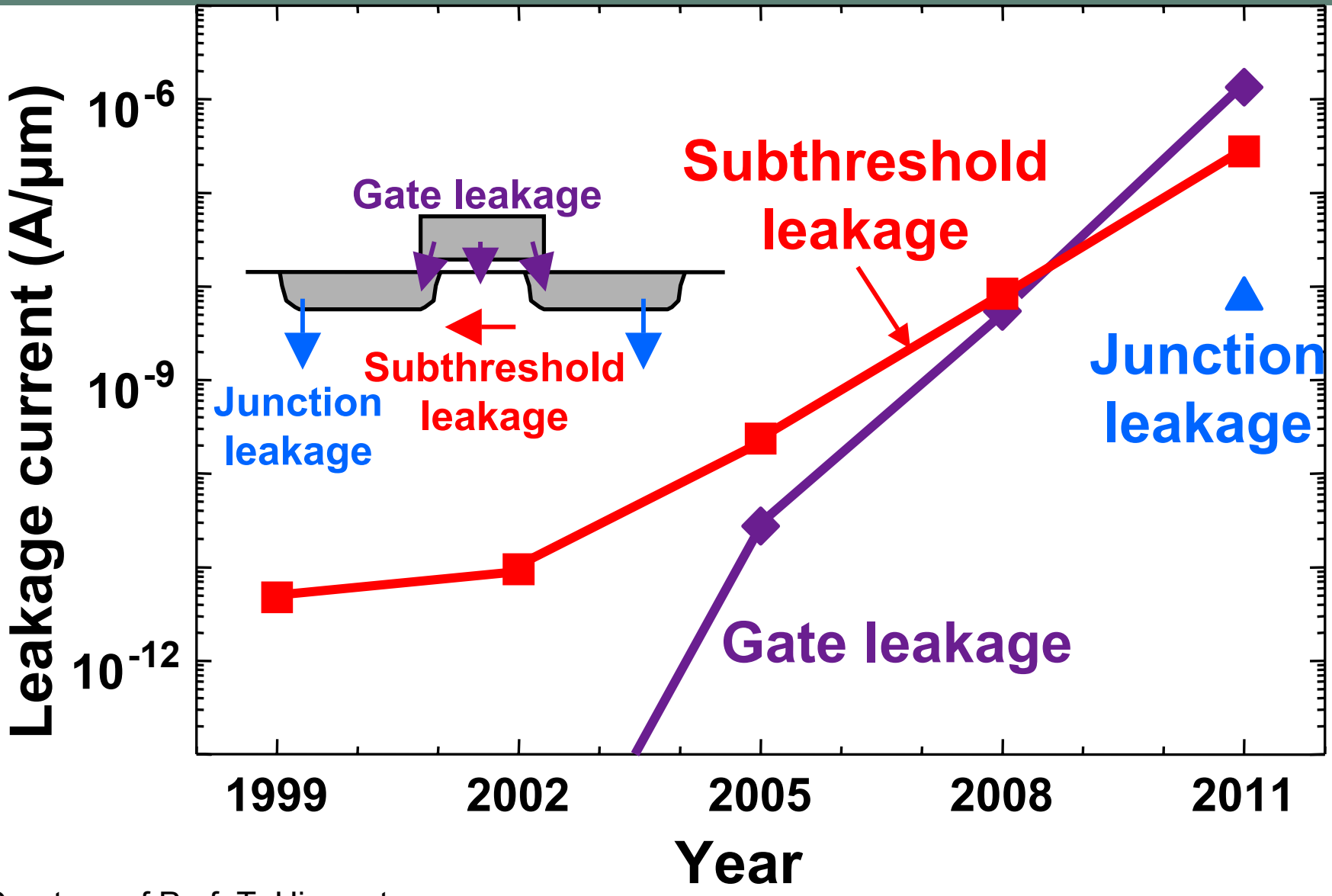
Crises in 90nm technology and beyond

Moore's law drives the industry for higher performance and lower cost but…

Ever increasing power consumption

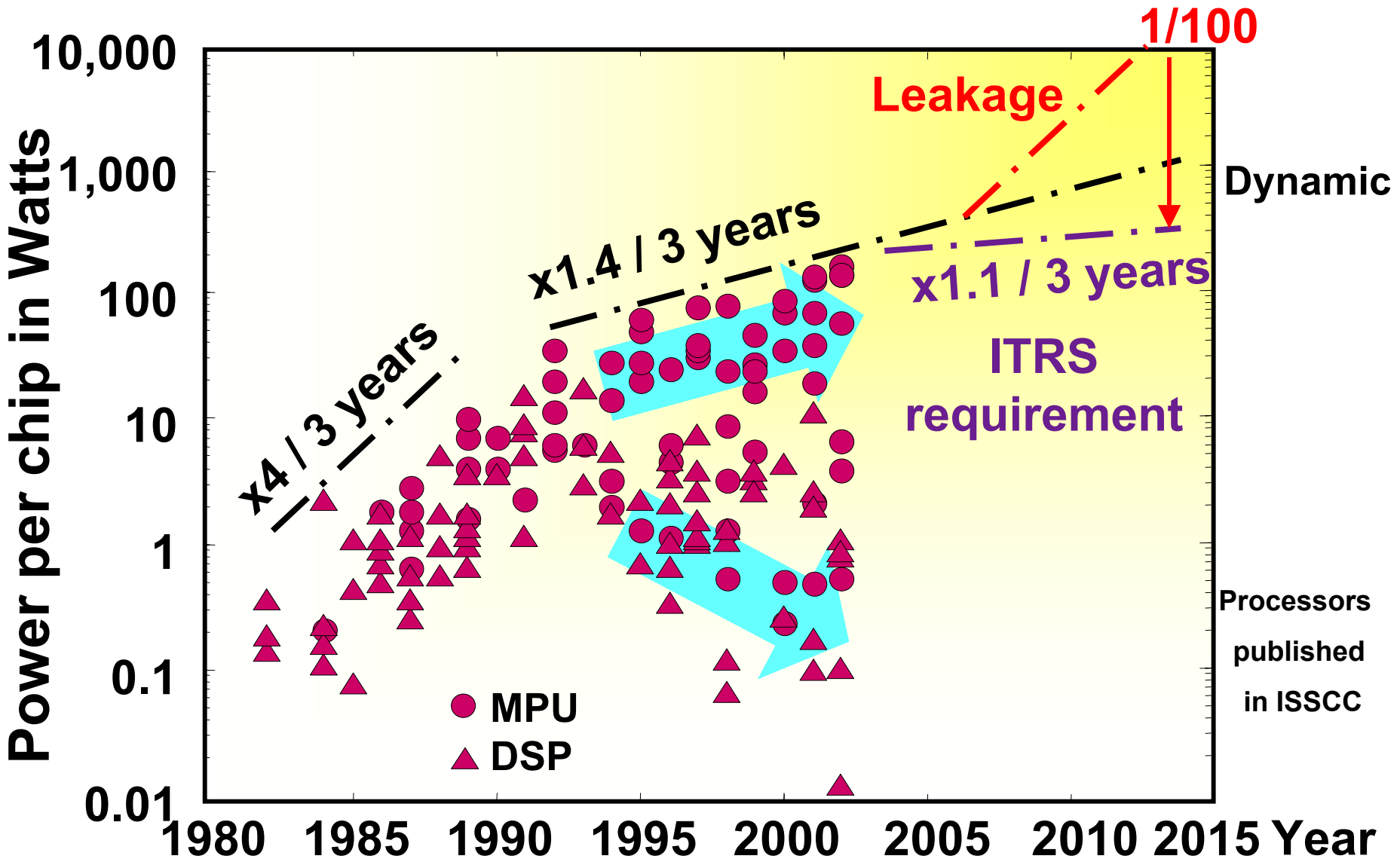


Transistors go leaky

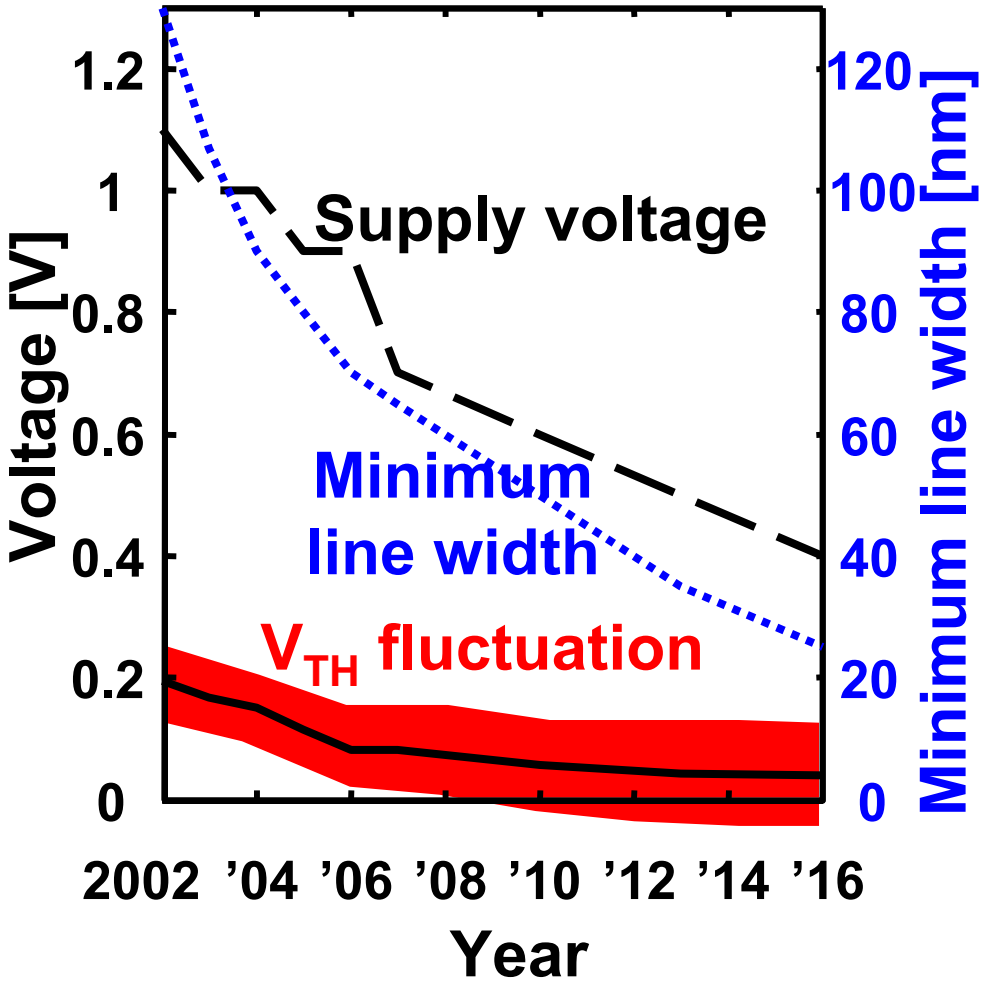


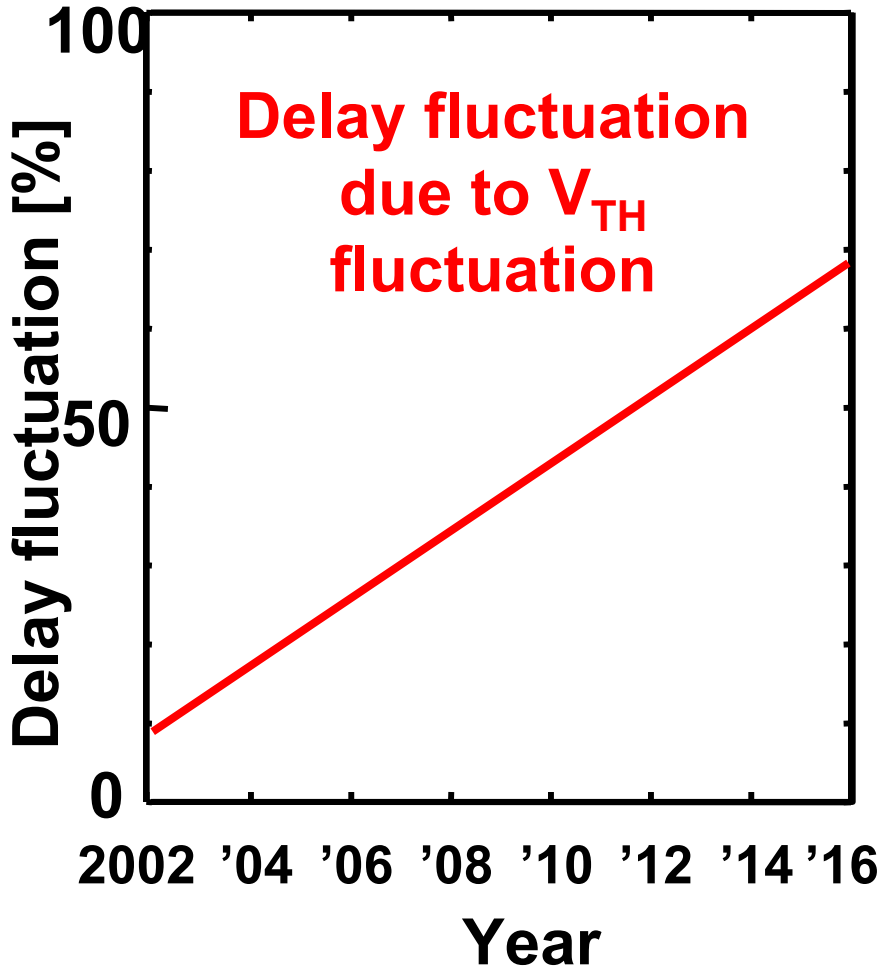
Courtesy of Prof. T. Hiramoto

Leakage may ruin Moore's law



V_{TH} Fluctuation is a real headache





→ **Lower yield & higher leakage**

Summary

Moore's law drives the industry for higher performance and lower cost but…

Leakage power explosion and V_{TH} fluctuation will be big stumbling blocks for Moore's law.

LongRun2 Technology Preview

Efficeon Launch Presentation

Leakage Challenges "Moore's Law"

The single biggest challenge to the microprocessor industry as we scale into 90nm and 65nm technologies is how to control transistor leakage power.

Leakage is a big problem.

So far, there have been few satisfactory solutions.

Leakage power could be the fundamental limiter for "Moore's Law."

LongRun2 Technology Preview

Transmeta has developed a solution to the Leakage Problem.

LongRun2

Software Controlled Leakage Management

LongRun2 Technology Preview

January 2000: Transmeta introduced LongRun power management
- Software dynamically adjusts voltage and MHz
- Very effective at reducing active power
- LongRun led the industry for 3 years

October 14, 2003 : Transmeta previews LongRun2
- LongRun2 adds Software Controlled Leakage Management
- LongRun2 dynamically adjusts transistor Vt's to control Leakage Power
- LongRun2 will allow future versions of Efficeon to:
  - Reduce leakage power while running
  - Reduce active power while running
  - Reduce standby power
- Efficeon already contains the necessary circuitry for LongRun2
  - Software, Hardware and CMOS process work together in this interdisciplinary solution to the Leakage problem.
- LongRun2 is the next leap forward in power management.

Pre-Demo Transistor Leakage Review

Transistors turn on when the input voltage to the gate is above a certain value, i.e. the "Threshold Voltage" or Vt.

Usually Vt is about 1/2 to 1/5th of the power supply voltage.

Transistors with lower Vt switch faster, but have more leakage.

- If Vt too low, power is wasted.

Transistors with higher Vt have less leakage, but are slower.

- If Vt too high, MHz is lost.

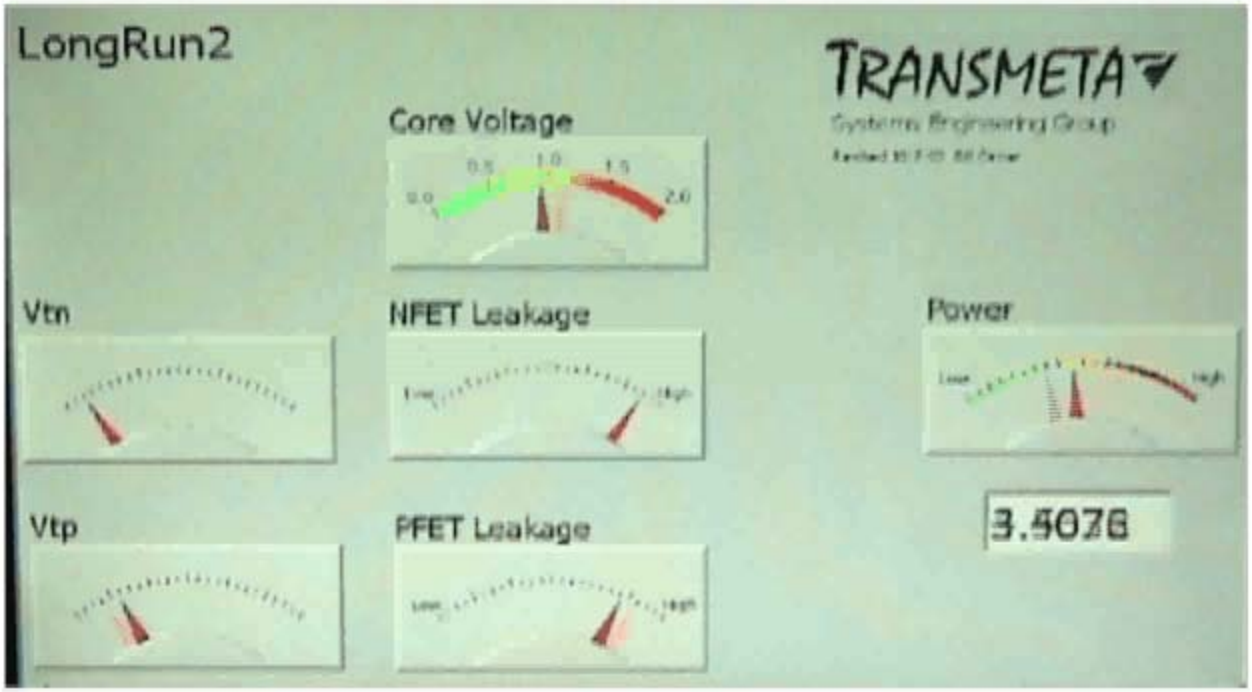
LongRun2 dynamically adjusts Vt for better efficiency.

Unwanted Vt fluctuations can be largely eliminated.

Efficeon LongRun2 Demonstration

LongRun2 Demo

Running Game



LongRun2 Technology Preview Summary

Summary of LongRun2 demonstration.

Efficeon's Code Morphing Software:

- Dynamically adjusted transistor Vt's while system was running to reduce excessive leakage and operate more efficently.
- In standby mode nearly all leakage power was eliminated.

Standby mode core power results:

- Leakage power in standby with LongRun2 disabled: 144 mW
- Leakage power in standby with LongRun2 enabled: 2 mW
- Leakage power reduced by ~70x with LongRun2

Special thanks to TSMC for fast cycle times and great yields.

LongRun2 will be announced in Efficeon products at a later time.

Safe Harbor Statement

This presentation includes certain forward-looking statements about our new products, roadmaps and other matters. Such statements speak only as of the date of this presentation, and we will not necessarily update them or any other forward-looking statements. Such statements necessarily involve risks and uncertainty, and our actual results may differ materially from our present expectations for a variety of reasons.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